

Basics of SPI: Timing Requirements and Switching Characteristics

TIPL 6002

TI Precision Labs – Digital Communications

Presented by Alex Smith

Prepared by Joseph Wu

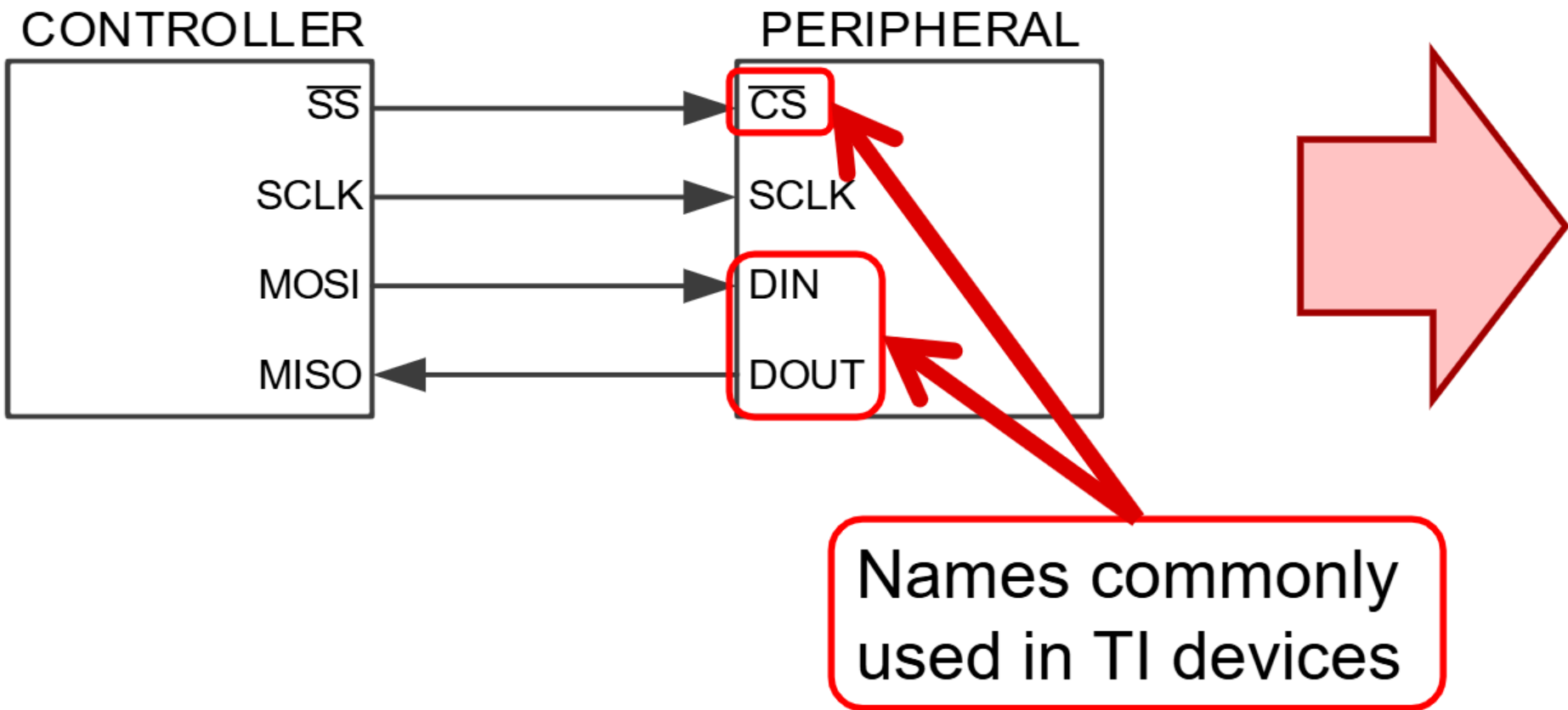
SPI 基础：时序要求和开关特性

TIPL 6002

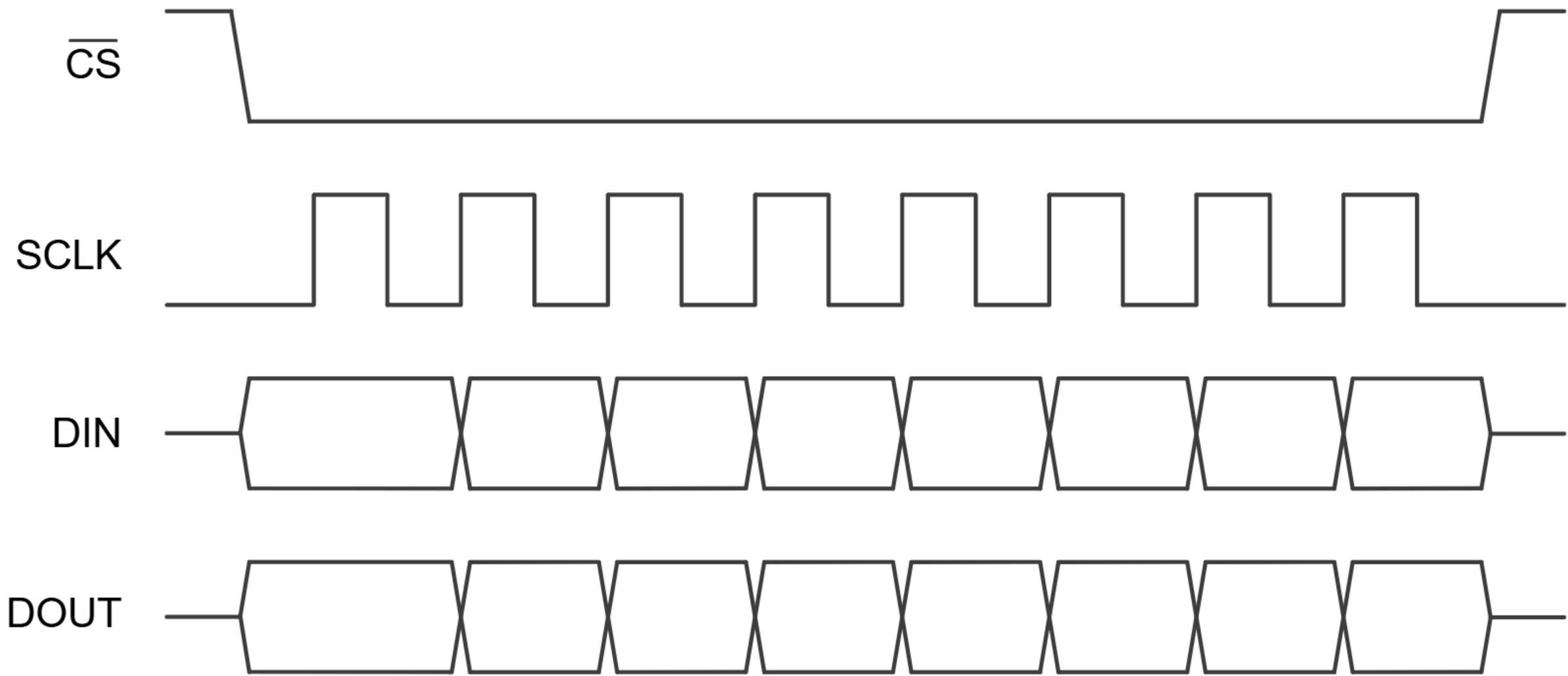
TI Precision Labs – 数字通信

由 Alex Smith 呈现 准备人：Joseph Wu

SPI Communication

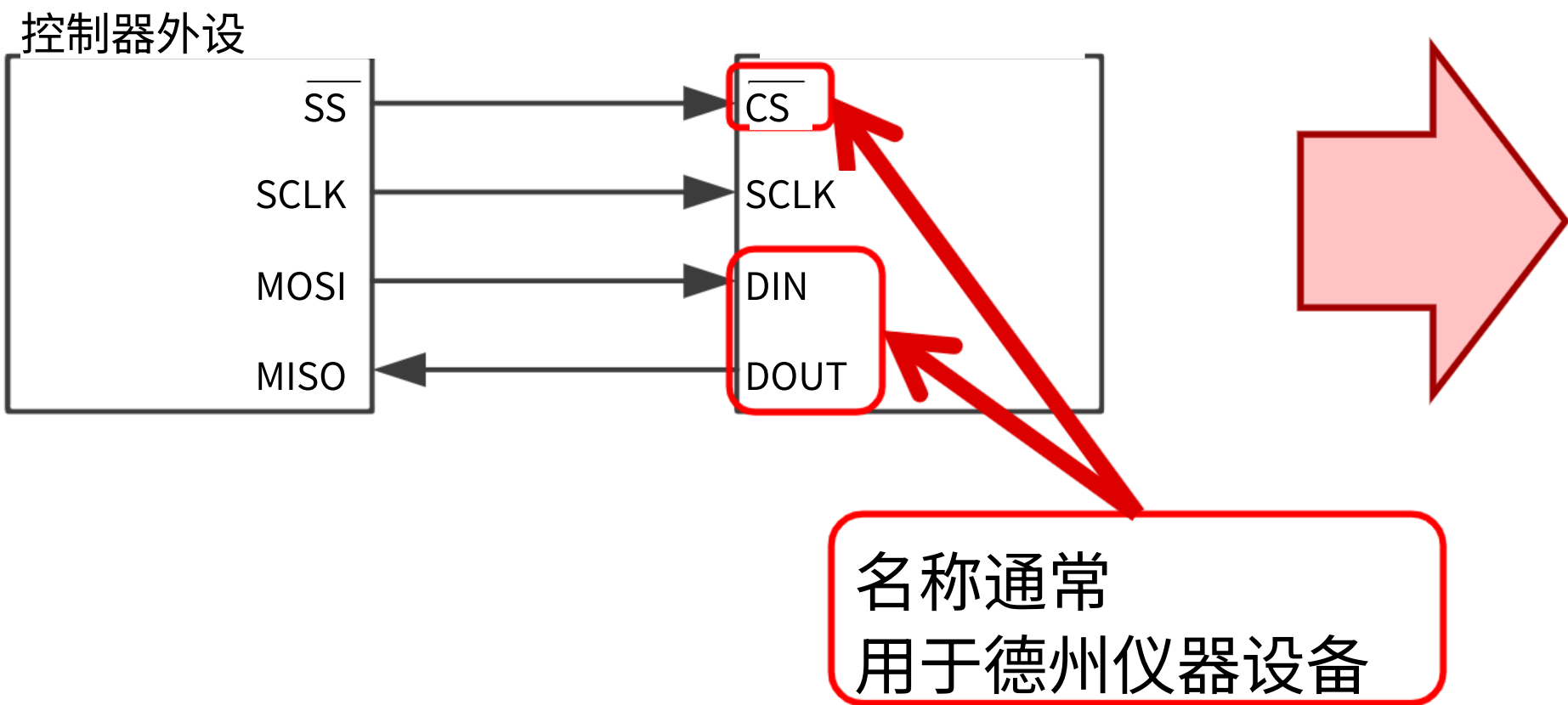


A timing diagram shows the specifications and the timing relationship between the SPI digital lines

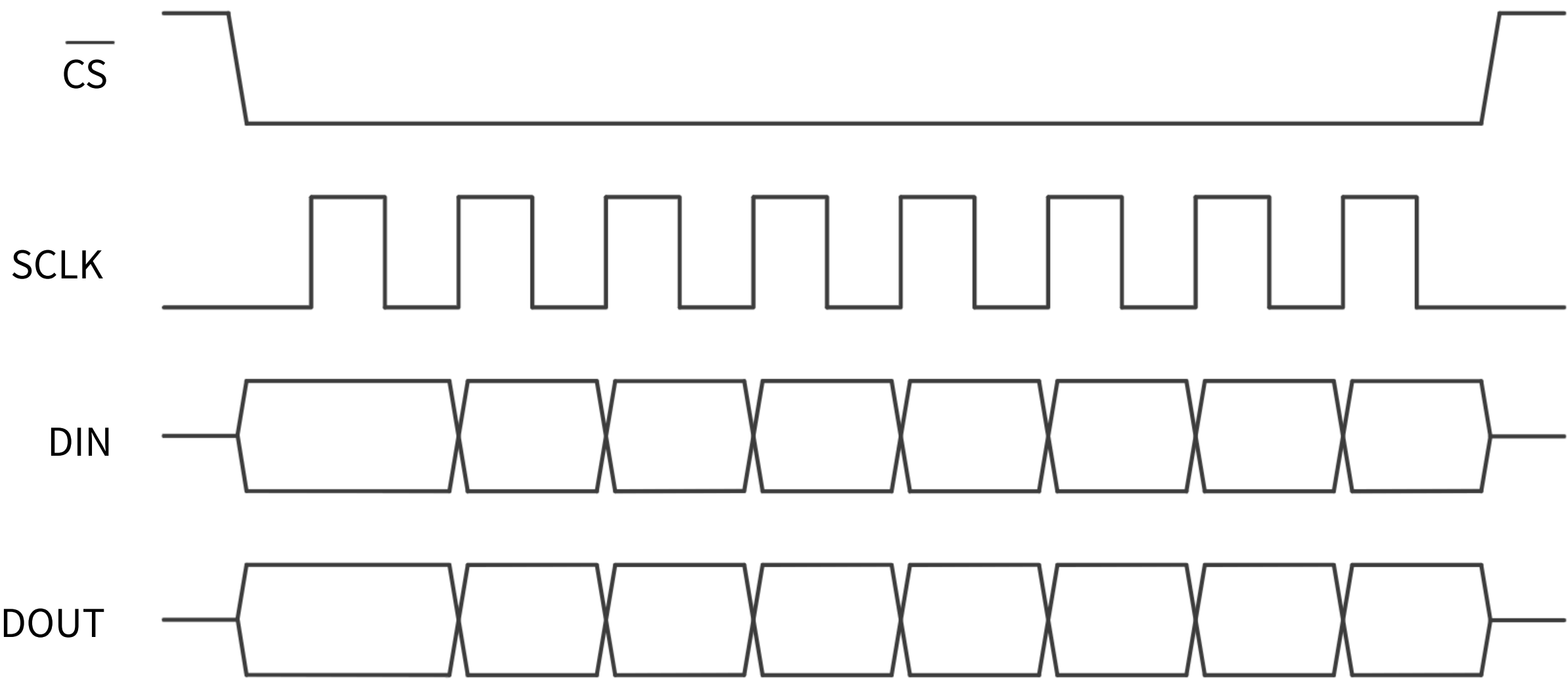


Violating a timing specification can cause a failure to read the data and may cause unexpected results.

SPI 通信

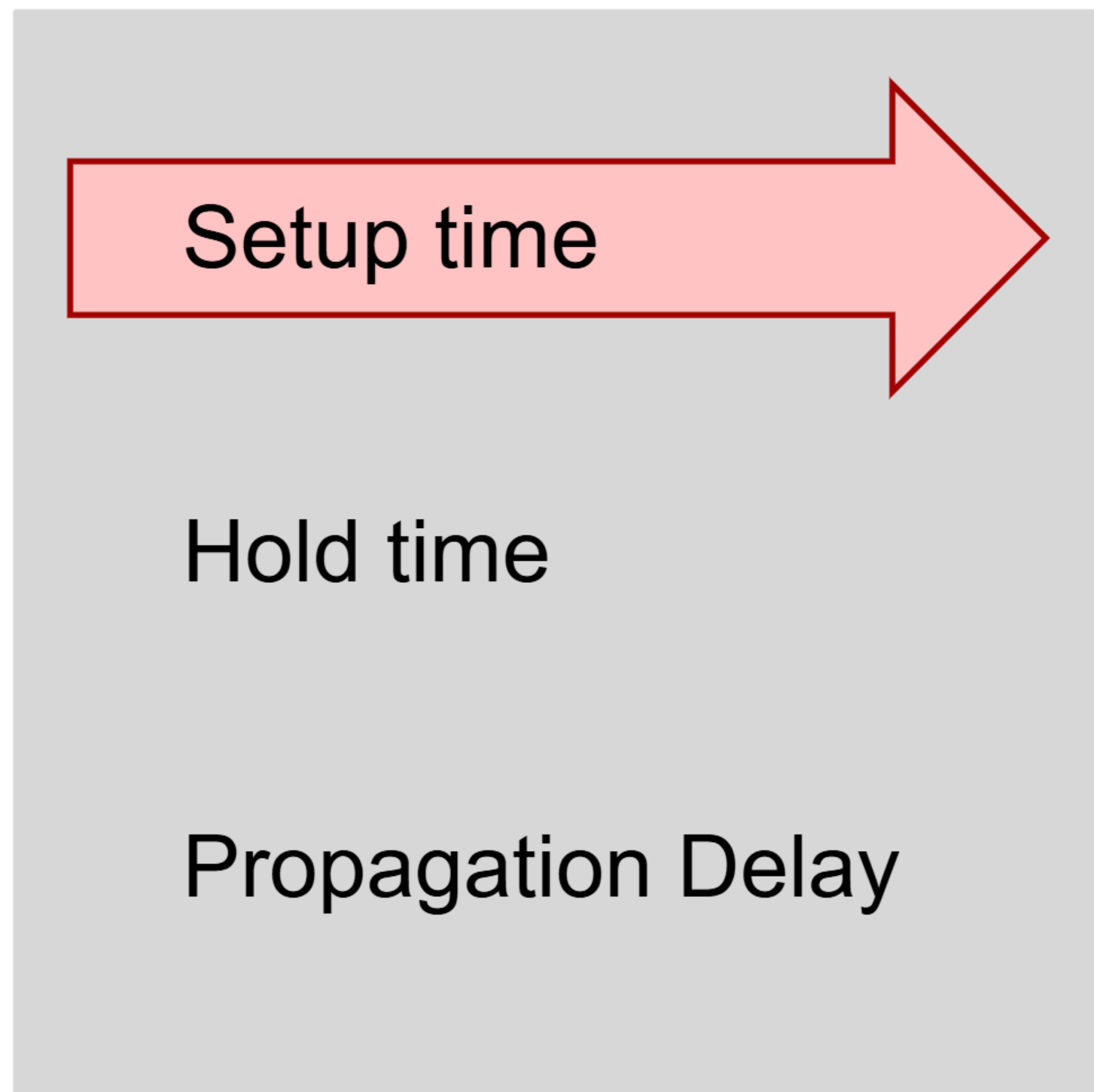


时序图显示了 SPI 数字线之间的规范和时序关系

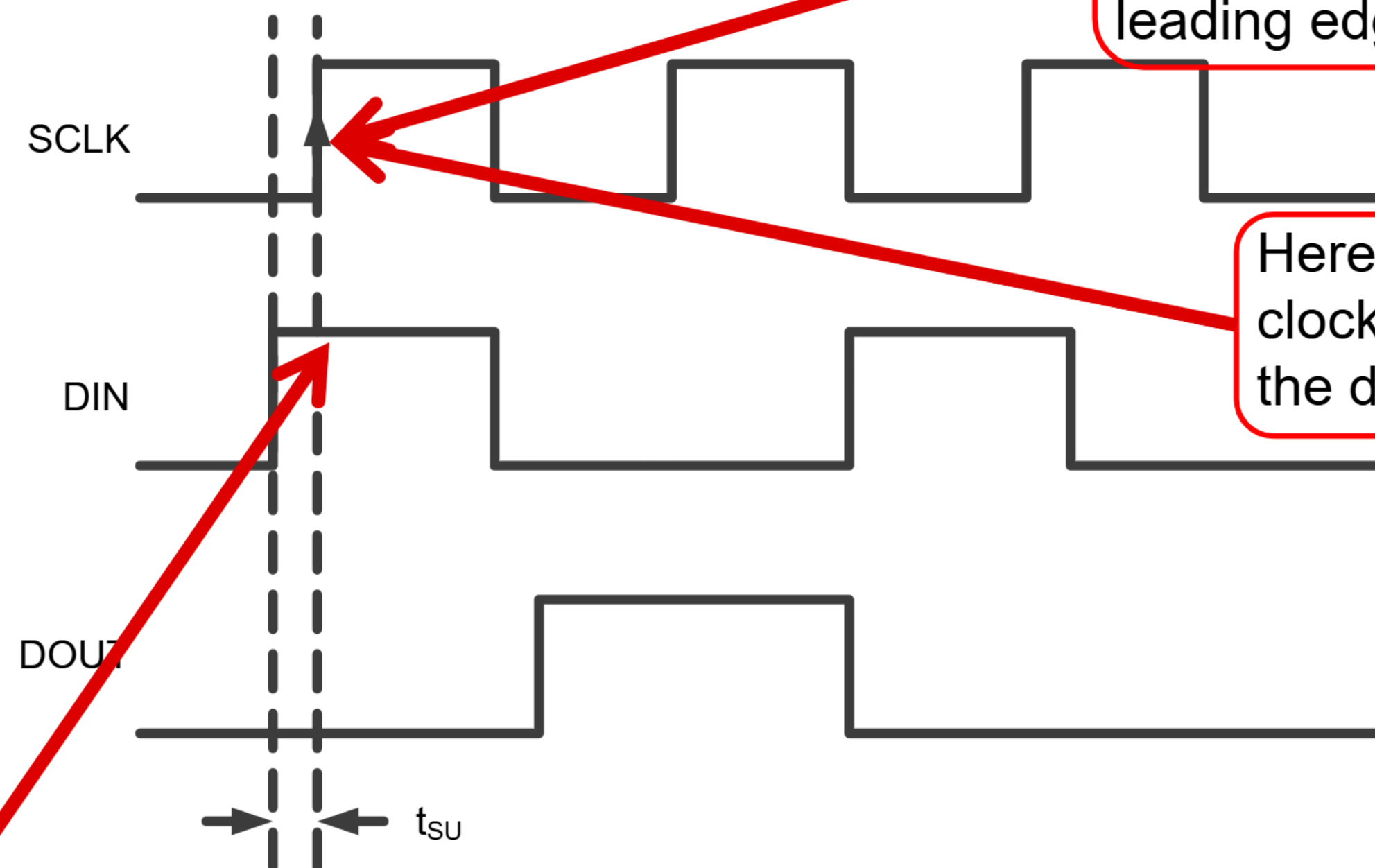


违反时序规范可能导致无法读取数据，并可能造成意外结果。

SPI Timing: Setup Time



The state of DIN is read into the device at the rising edge of SCLK. To ensure the data is correctly read, DIN must be at the correct state for a setup time **before** the SCLK rises

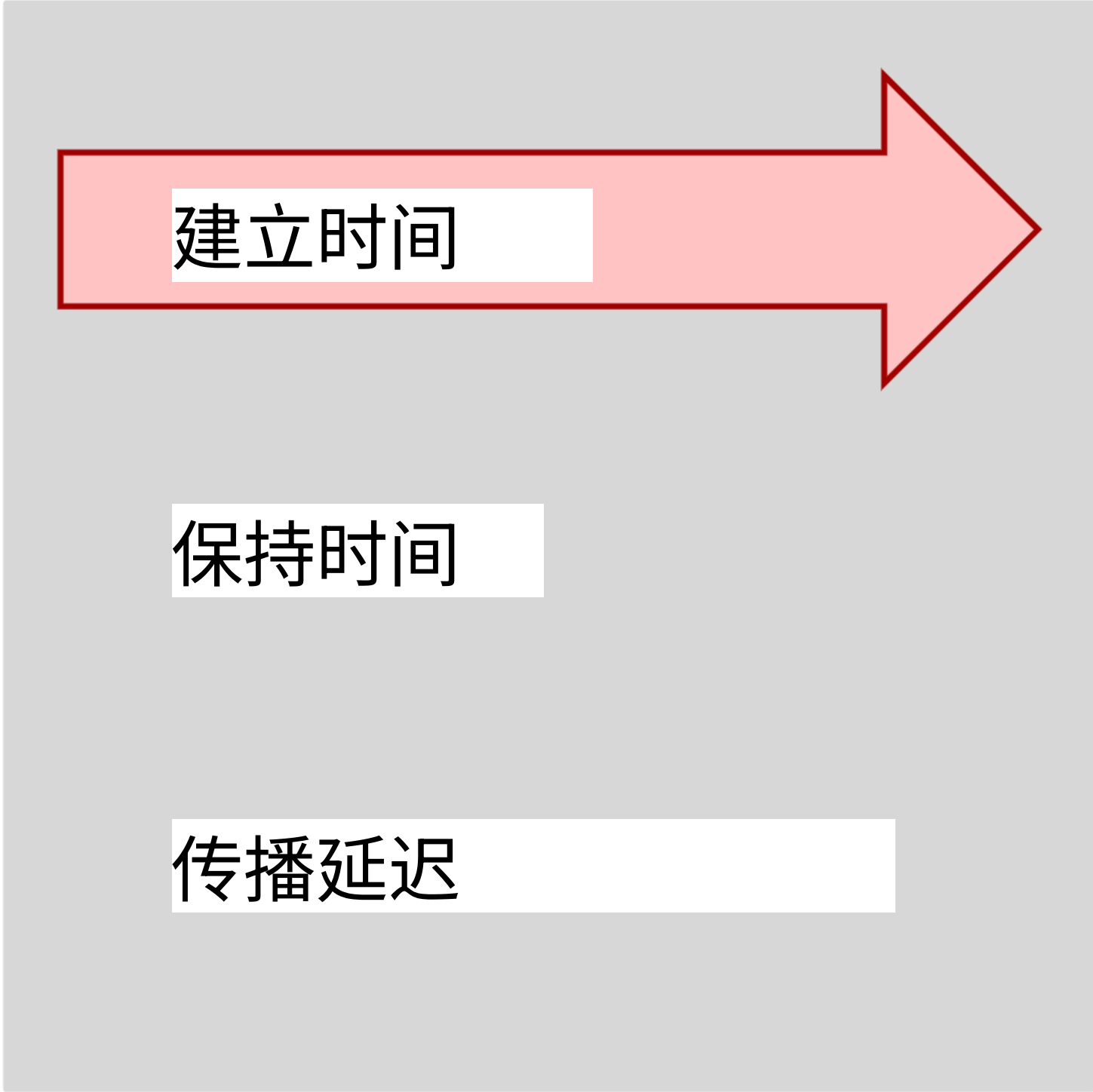


Example is SPI mode 0: SCLK idles low and data is clocked in on the leading edge of SCLK

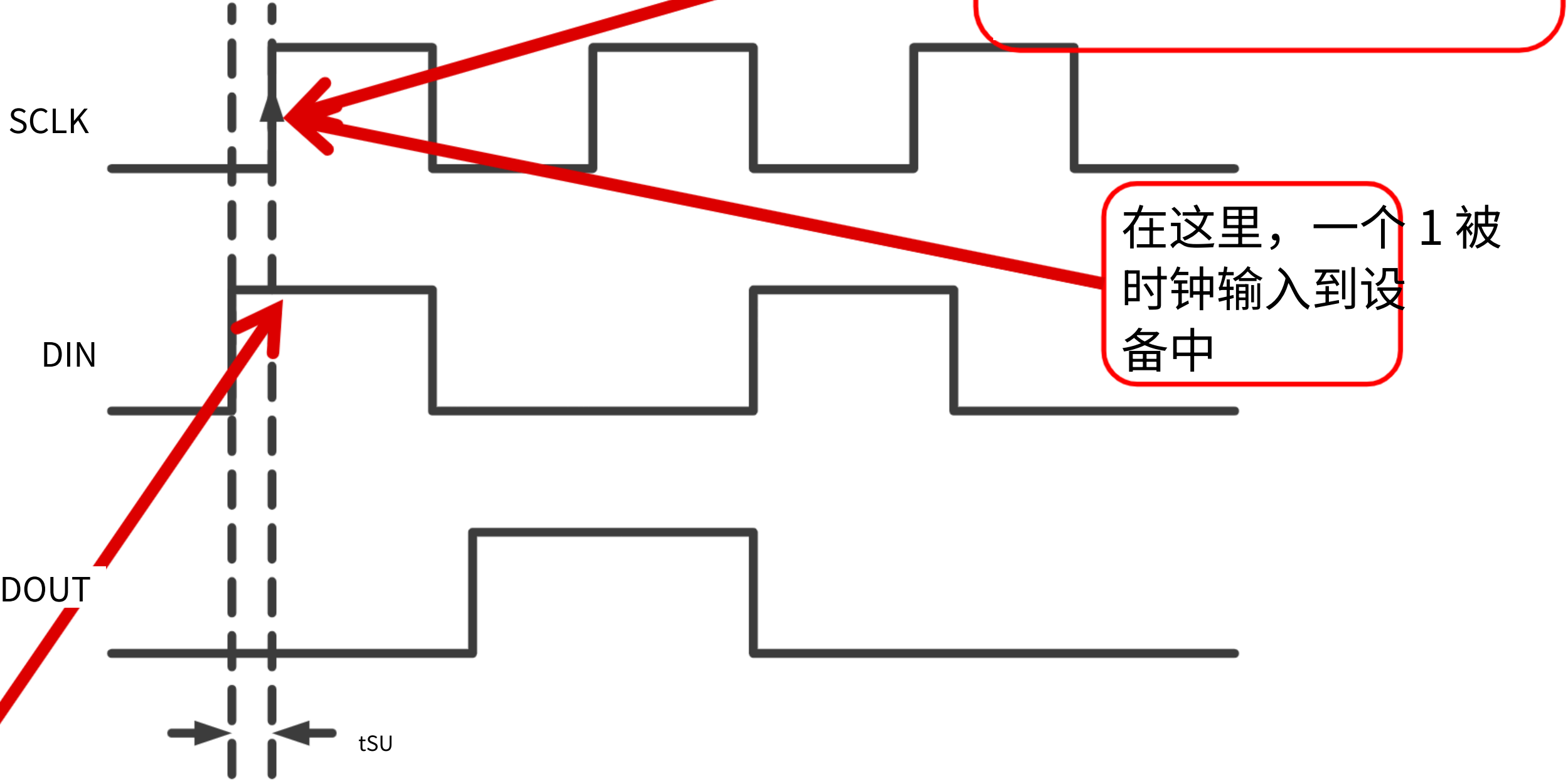
Here, a 1 is clocked into the device

Setup time is the minimum time required before the clocking edge for which the data must be stable to be latched correctly

SPI 时序：建立时间

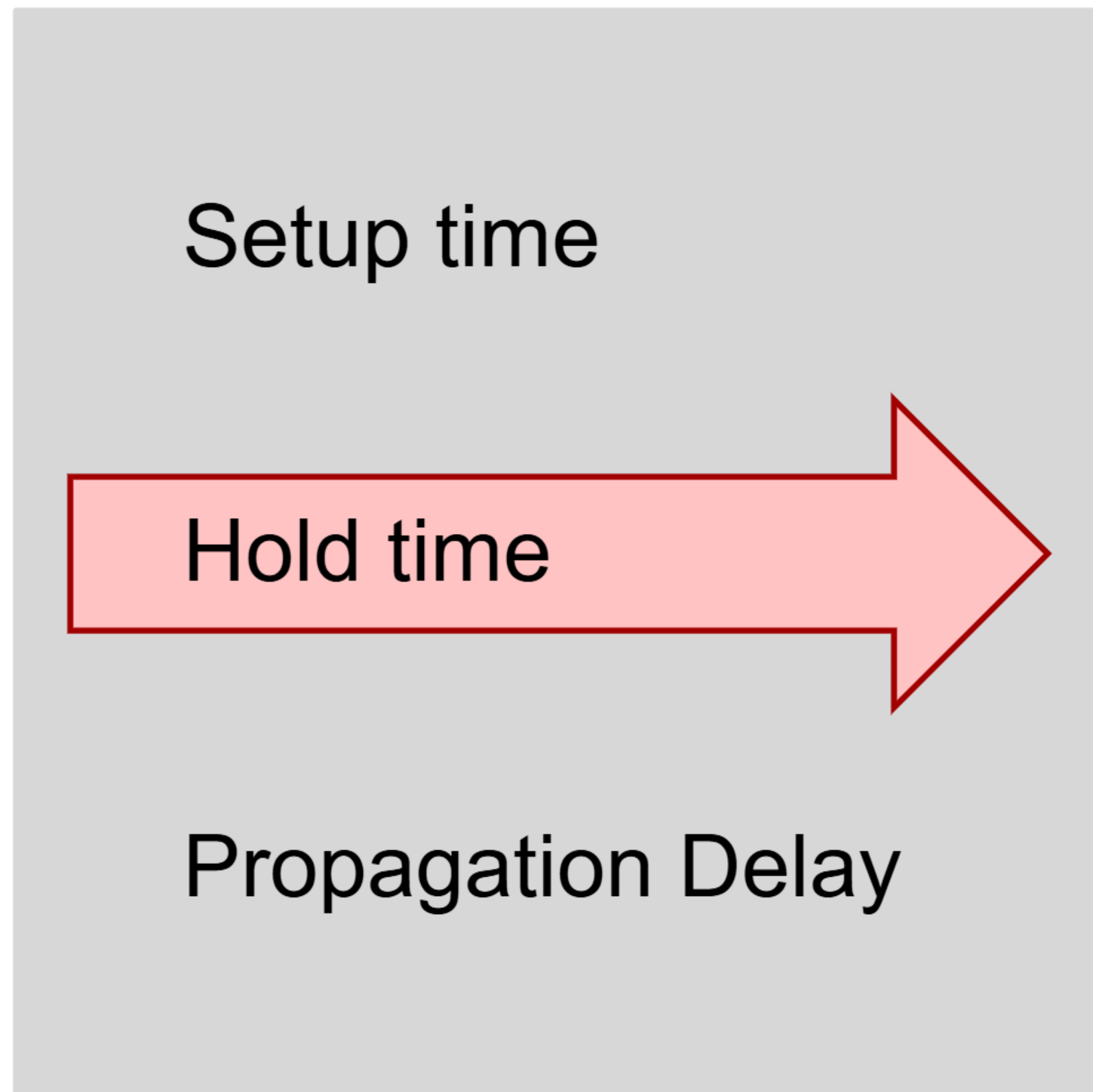


DIN 的状态在 SCLK 上升沿被读入设备。为确保数据正确读取，DIN 必须在 SCLK 上升前的建立时间内处于正确状态

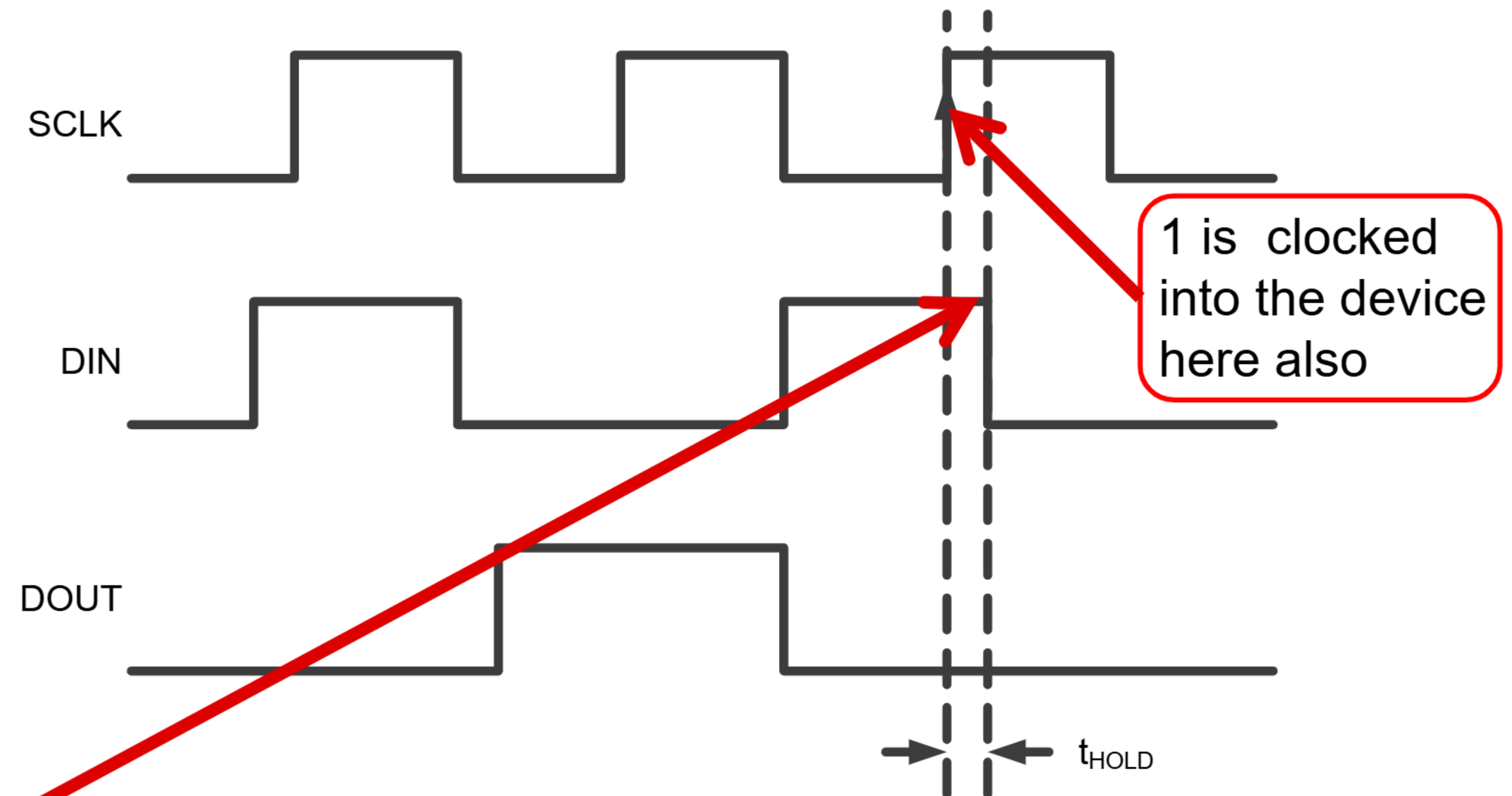


建立时间是在时钟边沿之前必须保持稳定的最短时间，以确保数据能够正确锁存

SPI Timing: Hold Time

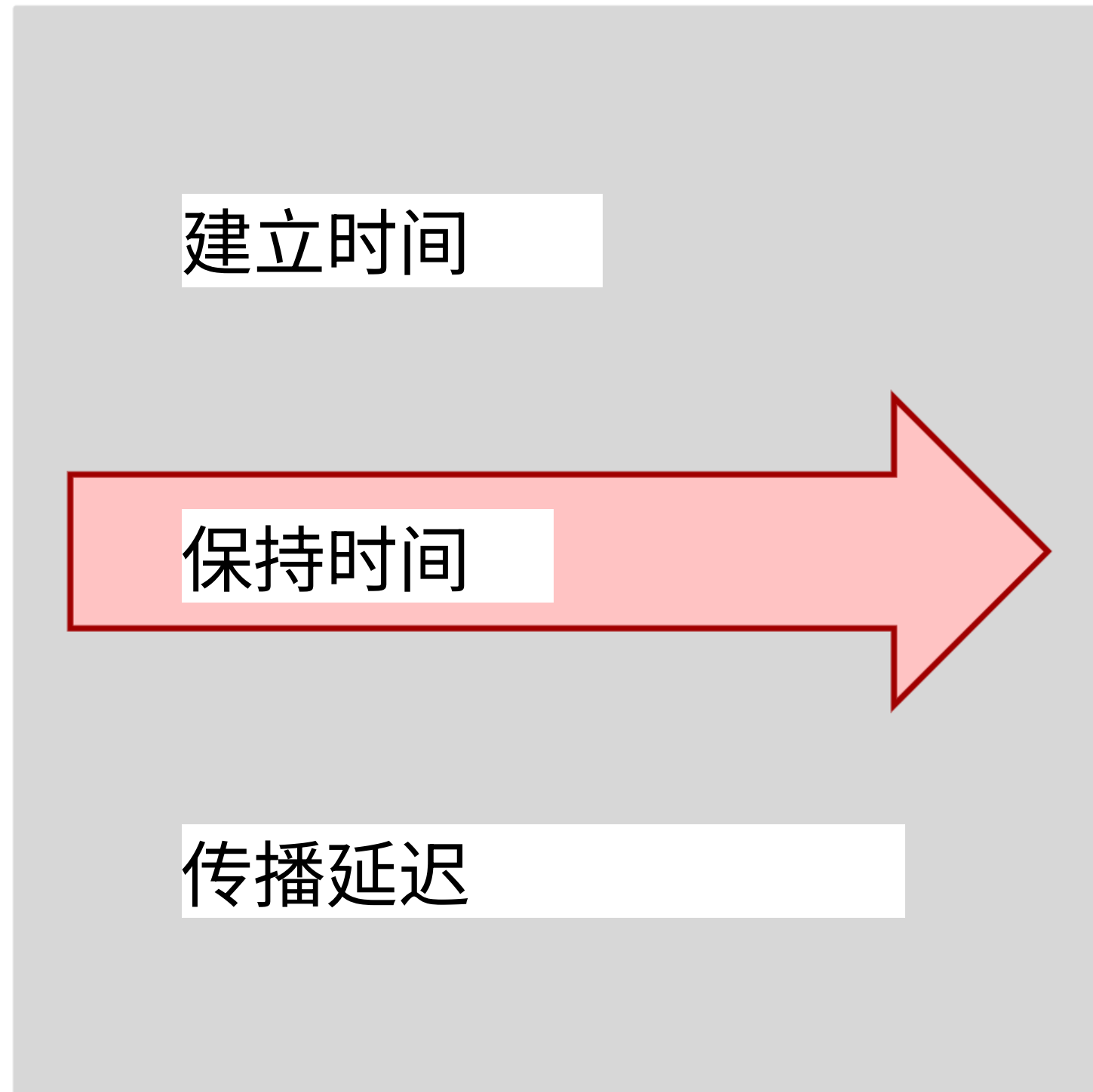


Again, the state of DIN is read into the device at the rising edge of SCLK. DIN must be held at the correct state for a hold time **after** the SCLK rises

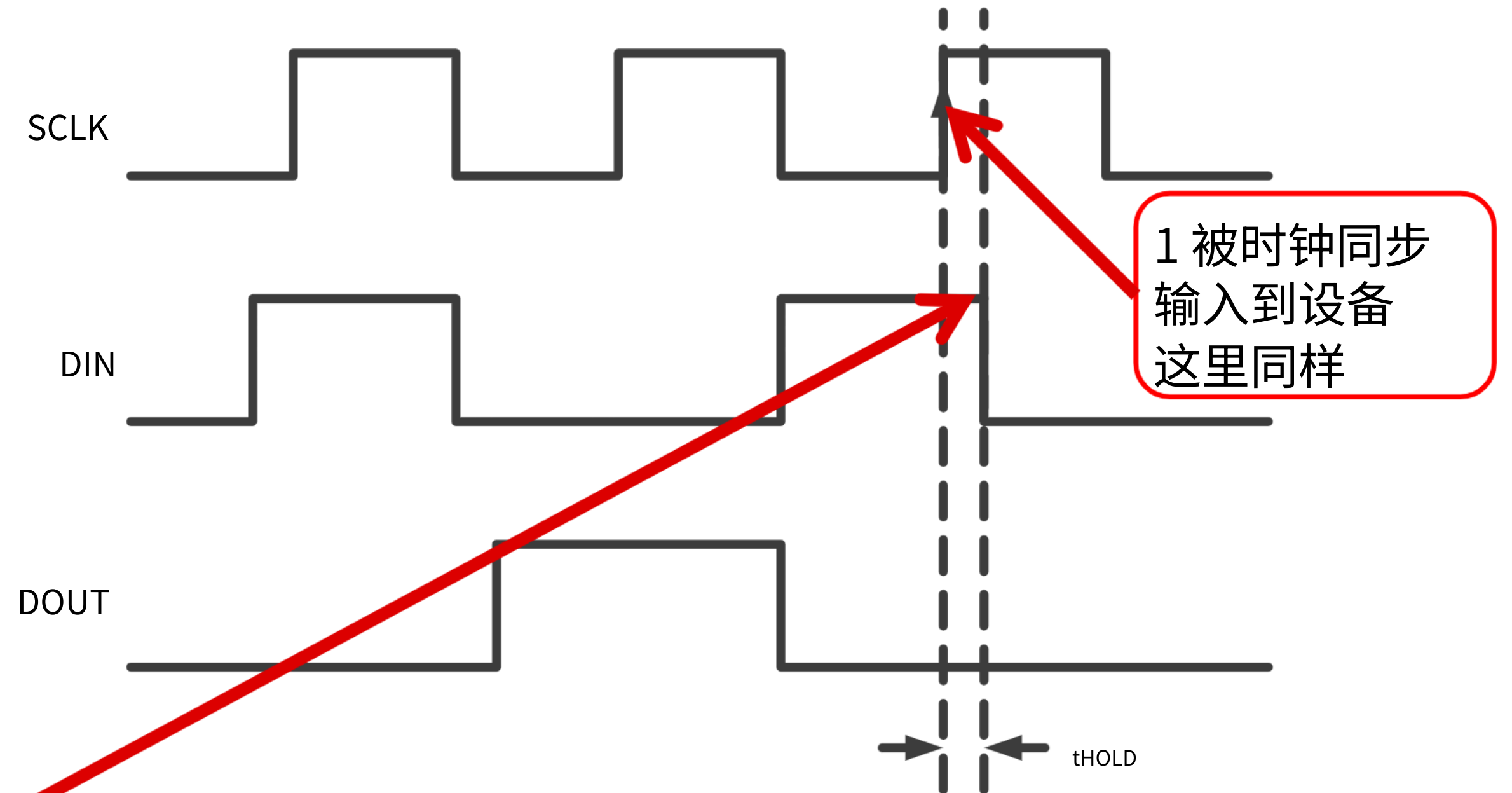


Hold time is the minimum time required after the clocking edge for which the data must be stable to be latched correctly

SPI 时序：保持时间

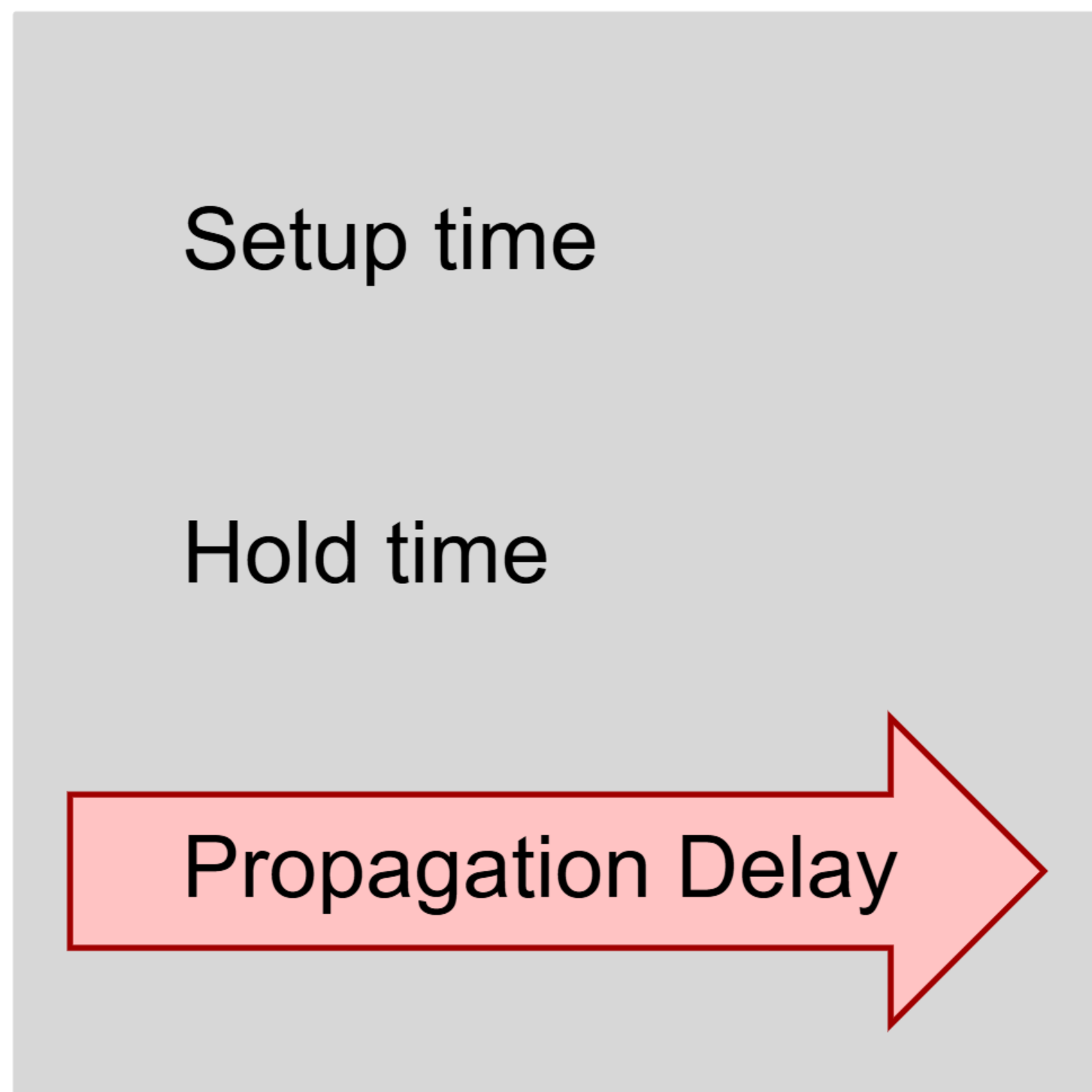


为确保数据被正确读取 再次，在 SCLK 的上升沿将 DIN 的状态读入设备中。SCLK 上升后，DIN 必须保持正确的状态一段时间（保持时间）

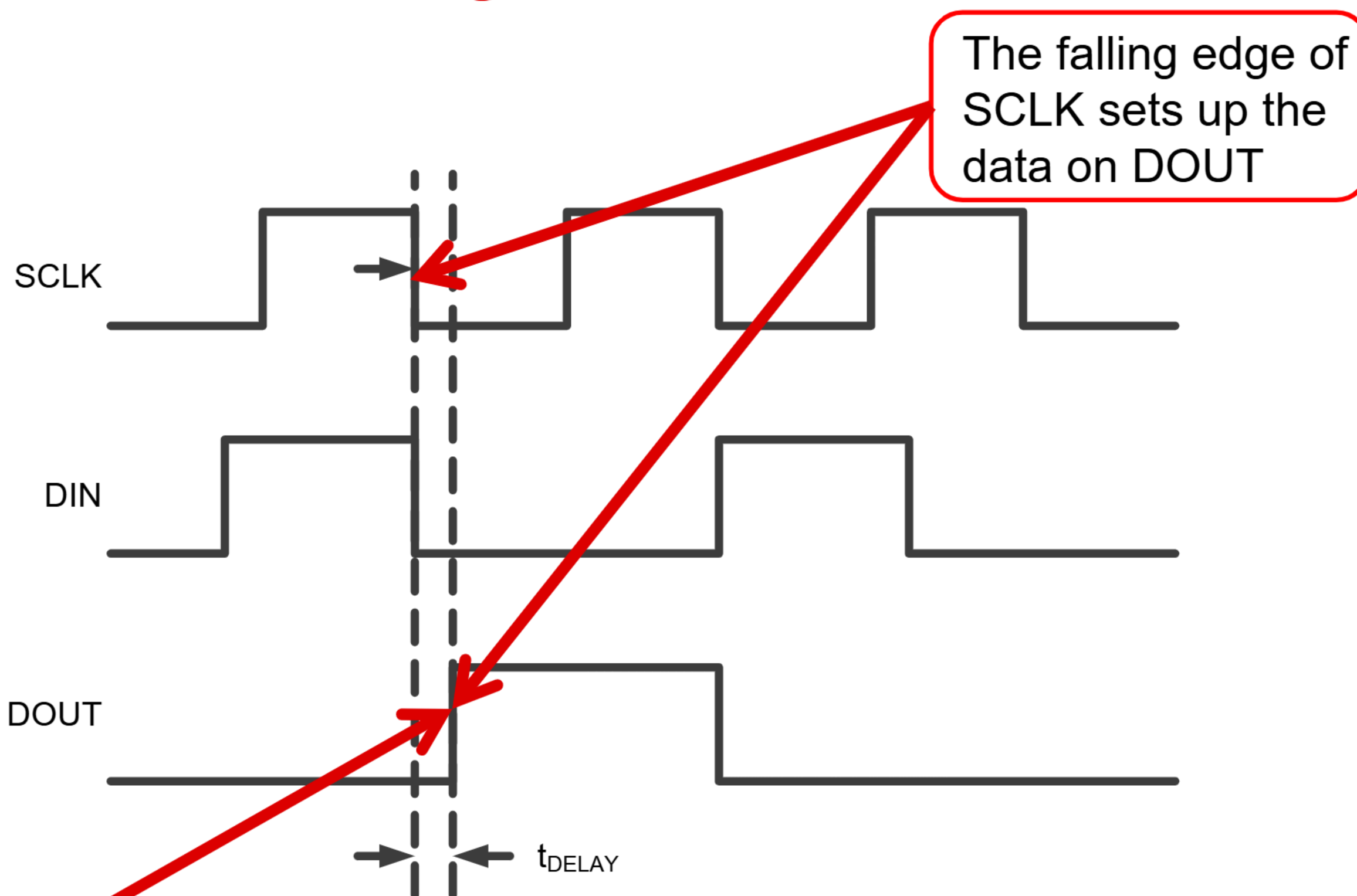


保持时间是指时钟边沿之后所需的最短时间，在此时间内数据必须保持稳定以确保正确锁存

SPI Switching: Propagation Delay

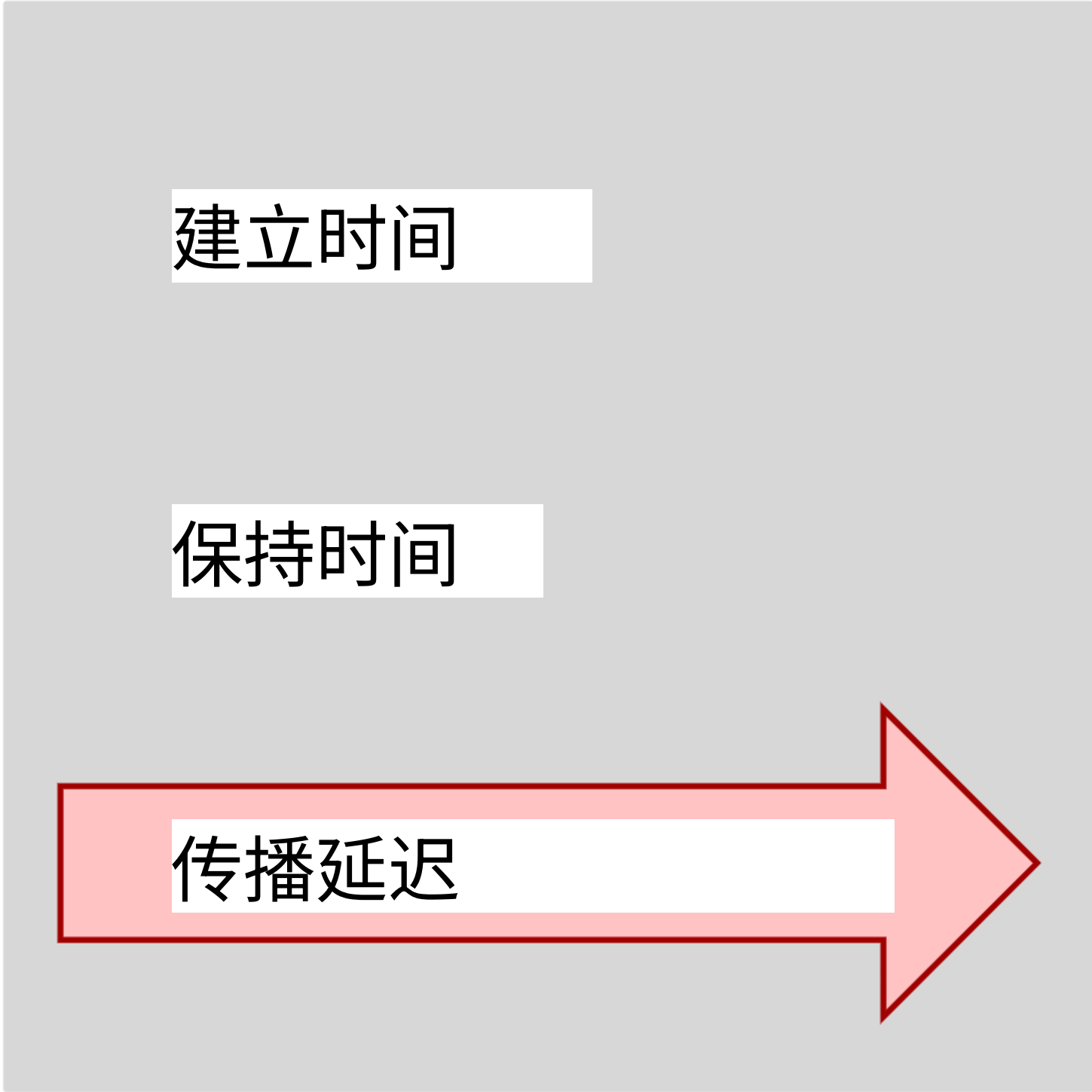


DOUT is read by the controller at the rising edge of SCLK. However, the peripheral sets the output at the previous falling edge of SCLK. This delay from one clock event to the response is a propagation delay.

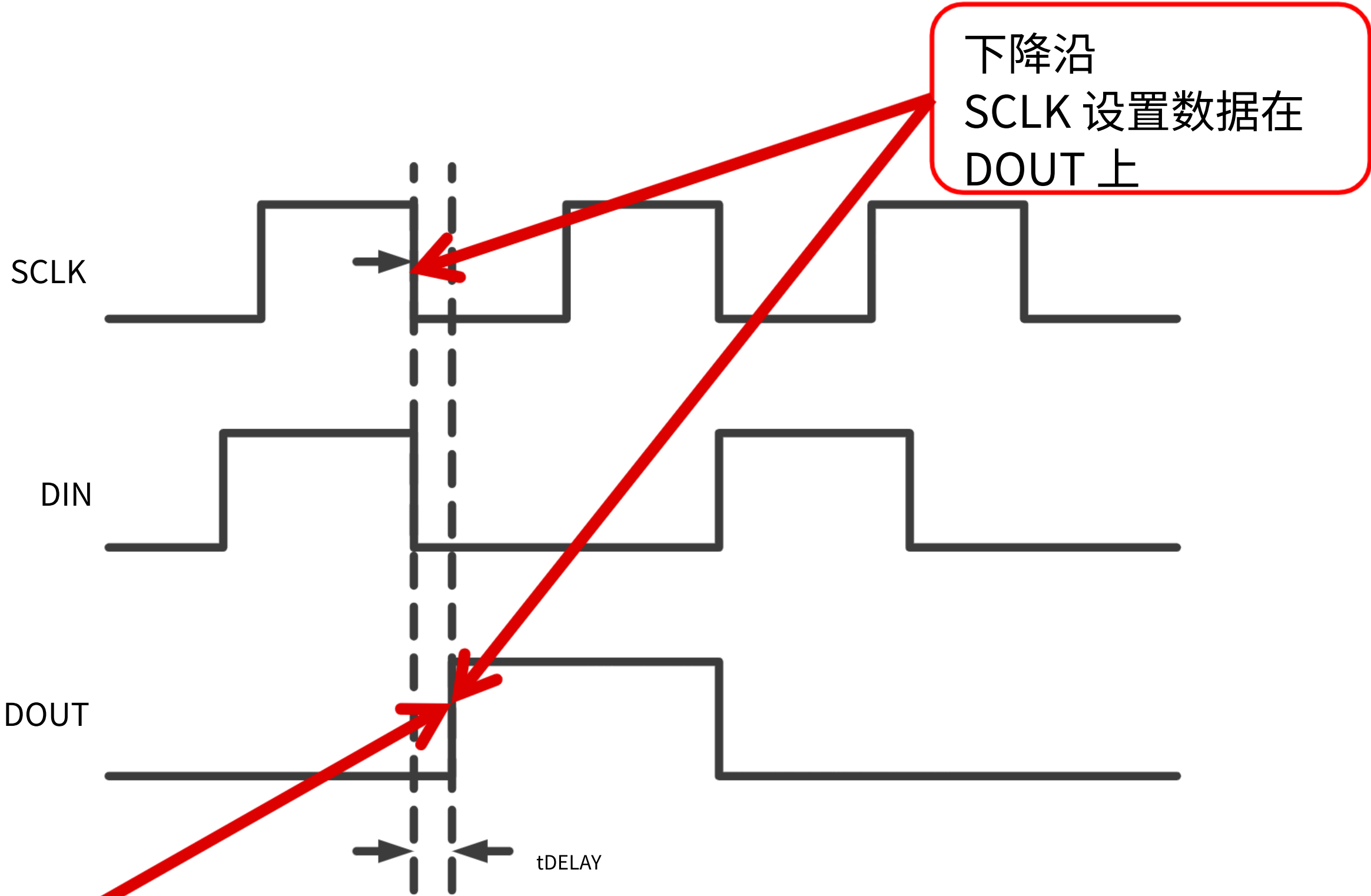


Propagation delay is the time required for an input change to cause an output change through the digital circuitry

SPI 切换：传播延迟



控制器在 SCLK 的上升沿读取 DOUT。然而，外设是在 SCLK 的前一个下降沿设置输出。从一个时钟事件到响应之间的延迟是传播延迟。



传播延迟是指输入变化导致数字电路输出变化所需的时间

SPI Timing

Timing Requirements and Switching Characteristics example from the ADS1118

Timing Requirements
are typically setup
times and hold times

7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t _{CSSC}	Delay time, $\overline{\text{CS}}$ falling edge to first SCLK rising edge ⁽¹⁾	100		ns
t _{SCCS}	Delay time, final SCLK falling edge to $\overline{\text{CS}}$ rising edge	100		ns
t _{CSH}	Pulse duration, $\overline{\text{CS}}$ high	200		ns
t _{SCLK}	SCLK period	250		ns
t _{SPWH}	Pulse duration, SCLK high	100		ns
t _{SPWL}	Pulse duration, SCLK low ⁽²⁾	100		ns
			28	ms
t _{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t _{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t _{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) $\overline{\text{CS}}$ can be tied low permanently in case the serial bus is not shared with any other device.

(2) Holding SCLK low longer than 28 ms resets the SPI interface.

Switching Characteristics
are typically propagation
delays

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{CSOOD}	Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT driven	DOUT load = 20 pF 100 kΩ to GND			100	ns
t _{DOPO}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF 100 kΩ to GND	0		50	ns
t _{CSDOZ}	Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT high impedance	DOUT load = 20 pF 100 kΩ to GND			100	ns

SPI 时序

时序要求
和切换
特性
来自示例
ADS1118

时序要求
通常是建立时间和保持时间

7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
t _{CSSC}	Delay time, $\overline{\text{CS}}$ falling edge to first SCLK rising edge ⁽¹⁾	100		ns
t _{SCCS}	Delay time, final SCLK falling edge to $\overline{\text{CS}}$ rising edge	100		ns
t _{CSH}	Pulse duration, $\overline{\text{CS}}$ high	200		ns
t _{SCLK}	SCLK period	250		ns
t _{SPWH}	Pulse duration, SCLK high	100		ns
t _{SPWL}	Pulse duration, SCLK low ⁽²⁾	100		ns
			28	ms
t _{DIST}	Setup time, DIN valid before SCLK falling edge	50		ns
t _{DIHD}	Hold time, DIN valid after SCLK falling edge	50		ns
t _{DOHD}	Hold time, SCLK rising edge to DOUT invalid	0		ns

- (1) $\overline{\text{CS}}$ can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.

开关特性通常是传播
延迟

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{CSDO}	Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT driven	DOUT load = 20 pF 100 kΩ to GND			100	ns
t _{DOPD}	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF 100 kΩ to GND	0		50	ns
t _{CSDOZ}	Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT high impedance	DOUT load = 20 pF 100 kΩ to GND			100	ns

SPI Timing Diagram

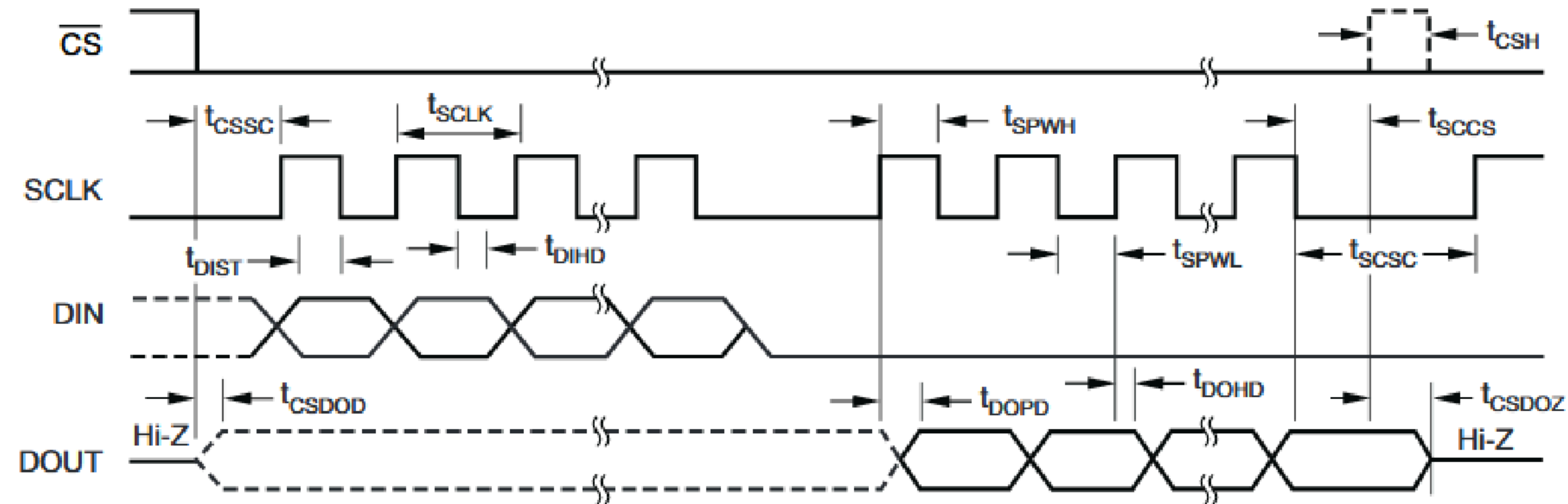


Figure 1. Serial Interface Timing

Timing diagram for the ADS1118

Device uses SPI Mode 1: SCLK idles low, data clocked in at falling edge of SCLK

Boxes for DIN and DOUT are high or low data

Arrows enclose timing specifications

SPI 时序图

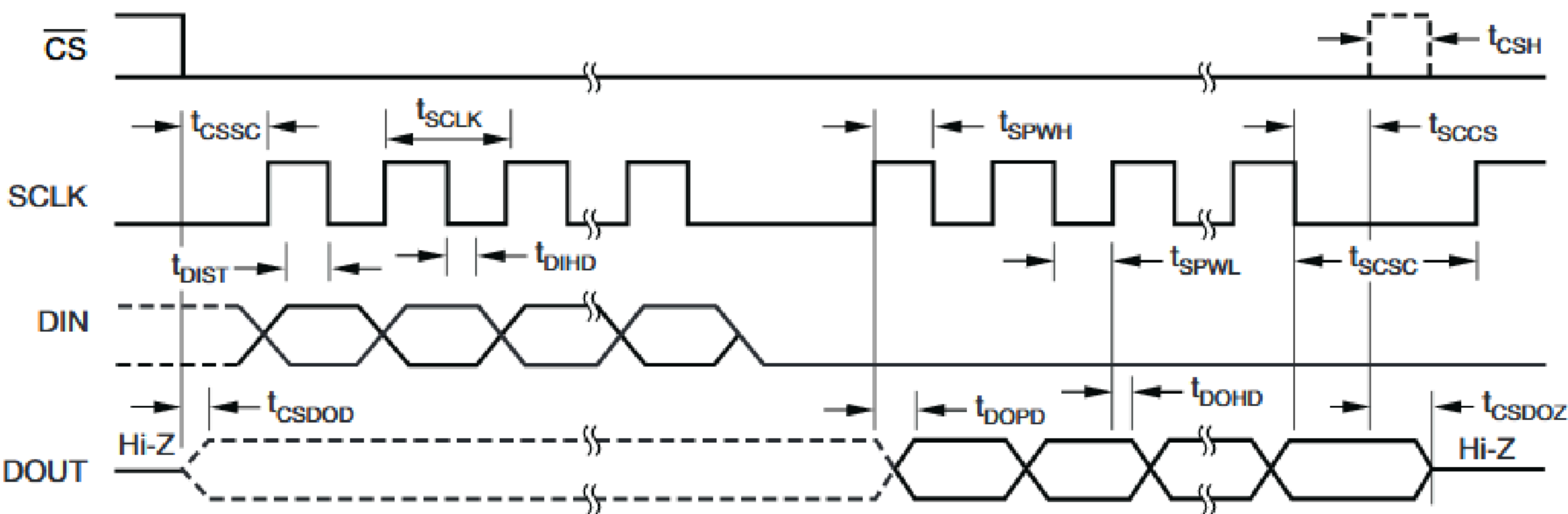


Figure 1. Serial Interface Timing

ADS1118 的时序图

设备使用 SPI 模式 1: SCLK 空闲低电平，数据在 SCLK 下降沿时钟输入 DIN 和 DOUT 的方框表示数据为高或低电平 箭头包围时序规范

SPI Timing Diagram

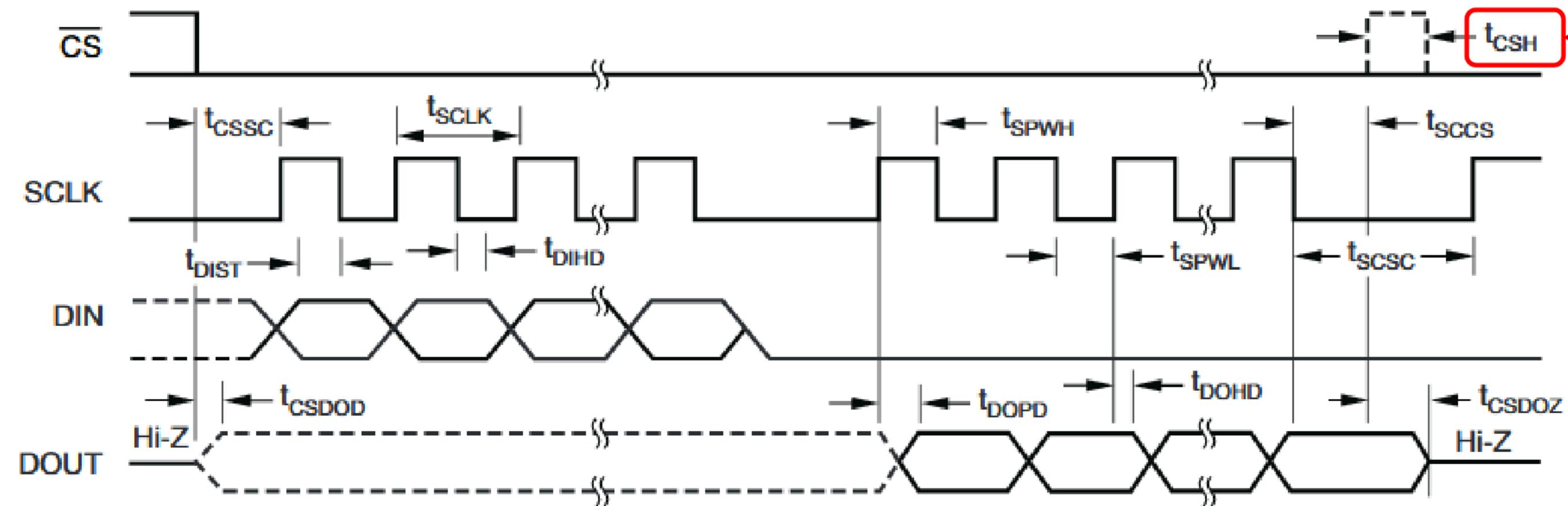


Figure 1. Serial Interface Timing

t_{CSH}

Minimum pulse duration, CS high

This time defines the time required for the CS to stay high to ensure that the device has reset the SPI communications.

SPI 时序图

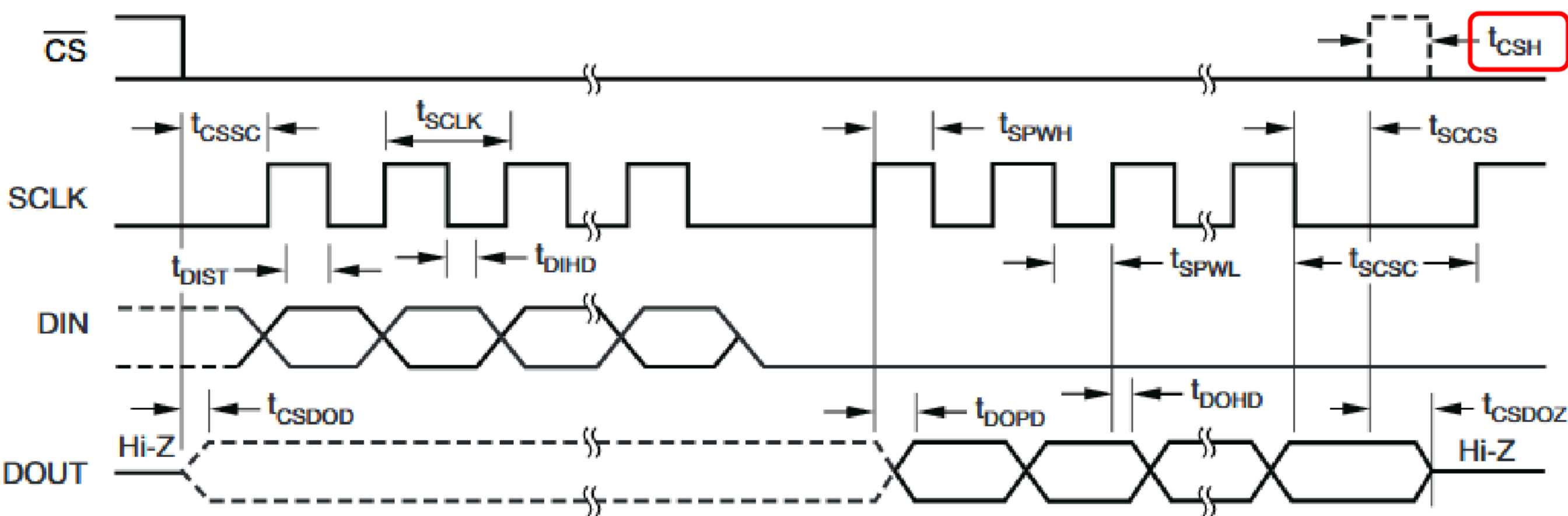


Figure 1. Serial Interface Timing

最小脉冲持续时间，CS 高
这个时间定义了 CS 需要保
持高电平的时间，以确保设
备重置了 SPI 通信。

SPI Timing Diagram

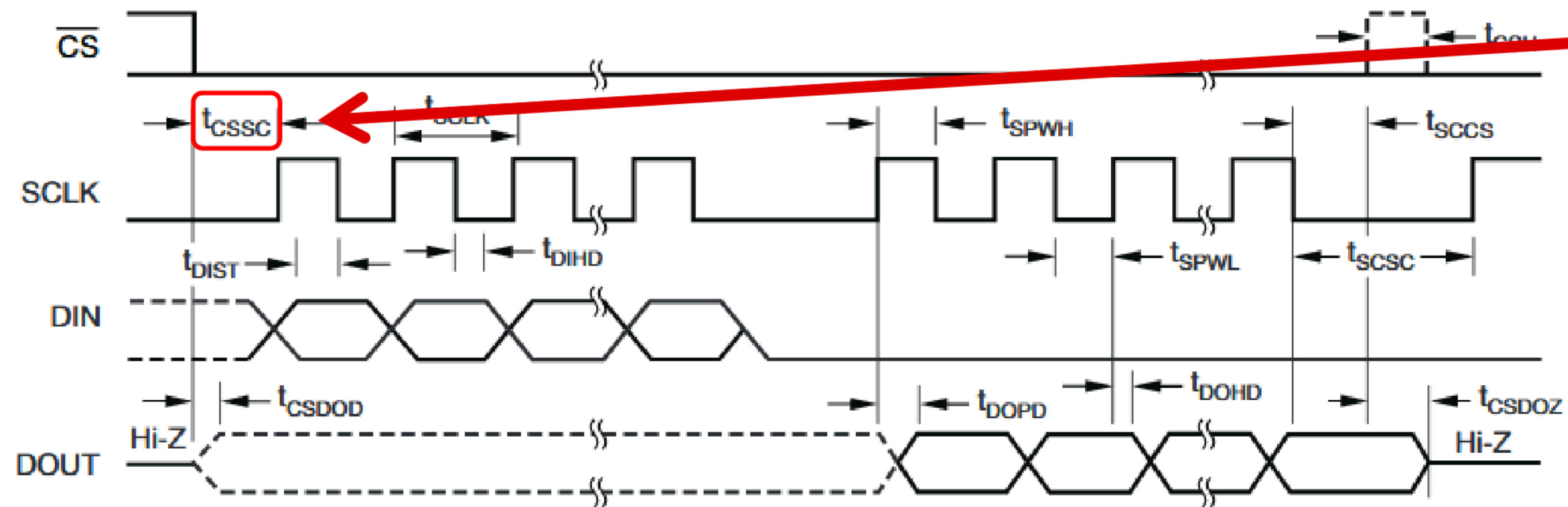


Figure 1. Serial Interface Timing

t_{CSSC}

CS low to first SCLK high

This time defines the time required for the CS to stay high to ensure that the device recognizes it is the peripheral.

A violation may cause the device to miss the first SCLK pulse

SPI 时序图

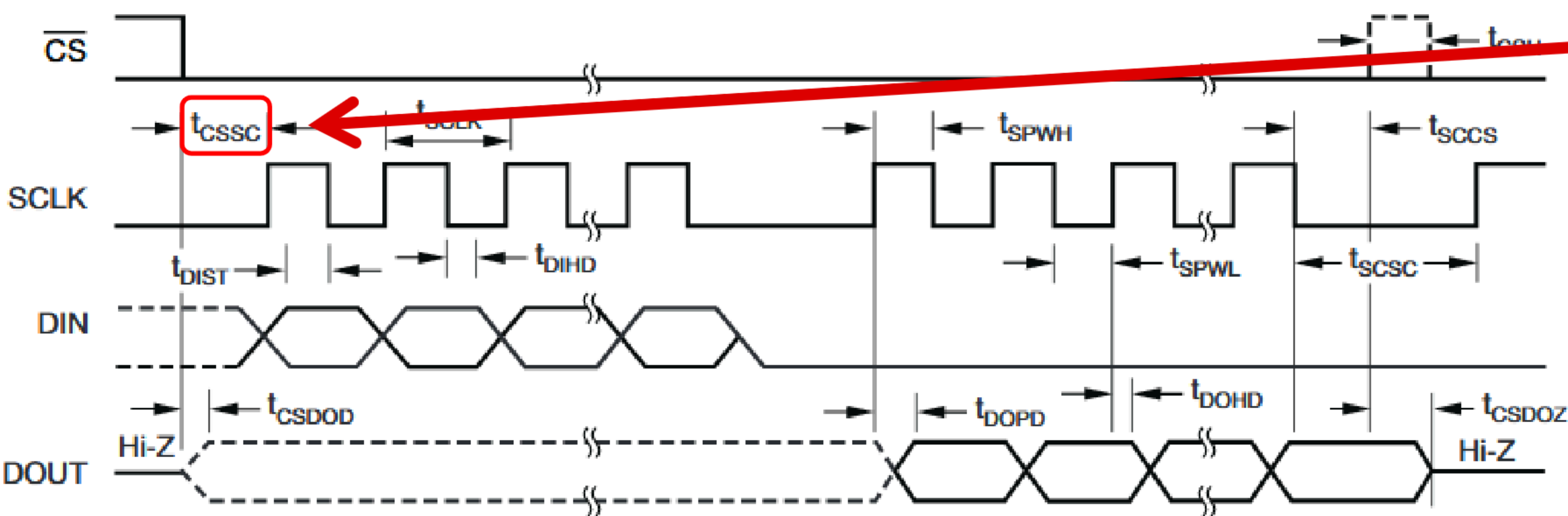


Figure 1. Serial Interface Timing

tCSSC

CS 低到第一个 SCLK 高 这段时间定义了 CS 需要保持高电平以确保设备识别其为外设的时间。违规可能导致设备错过第一个 SCLK 脉冲

SPI Timing Diagram

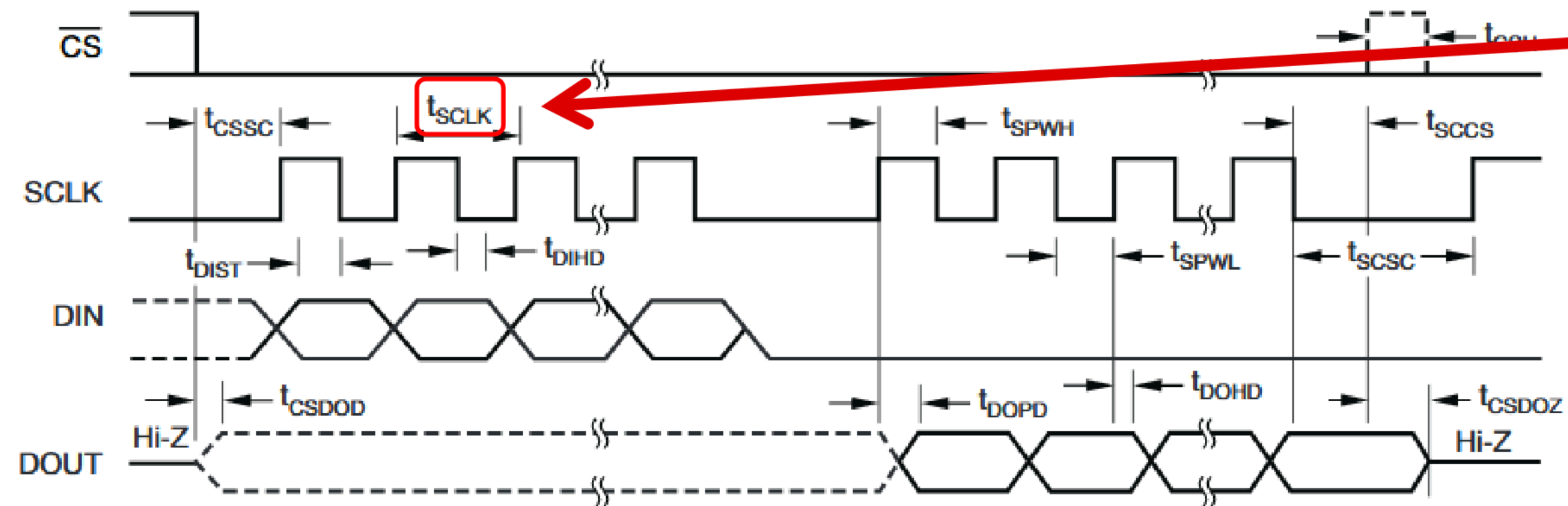


Figure 1. Serial Interface Timing

t_{SCLK}

The minimum time for an SCLK period

SCLKs can be sent to a device only so fast before the device fails to recognize it. This defines the minimum time for SCLK.

$1/t_{SCLK}$ is the SCLK frequency

SPI 时序图

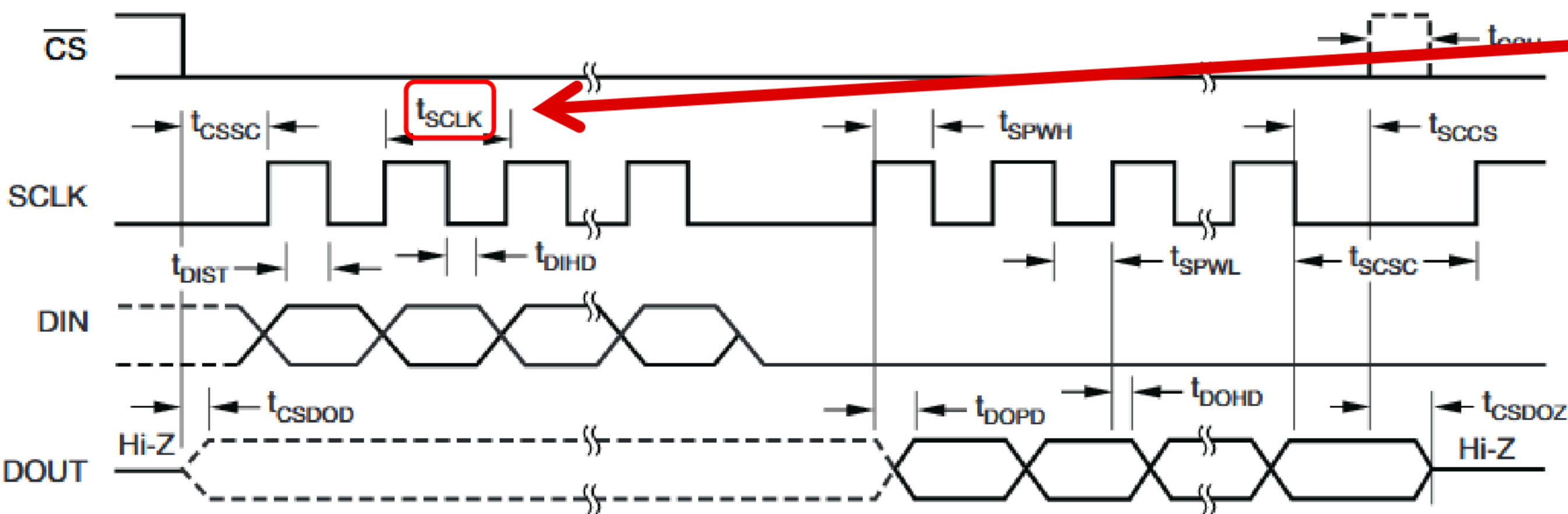


Figure 1. Serial Interface Timing

tSCLK

SCLK 的最小周期时间 SCLK 只能以这种方式发送到设备，否则设备将无法识别。这定义了 SCLK 的最小时间。1/t 即为 SCLK 频率

SPI Timing Diagram

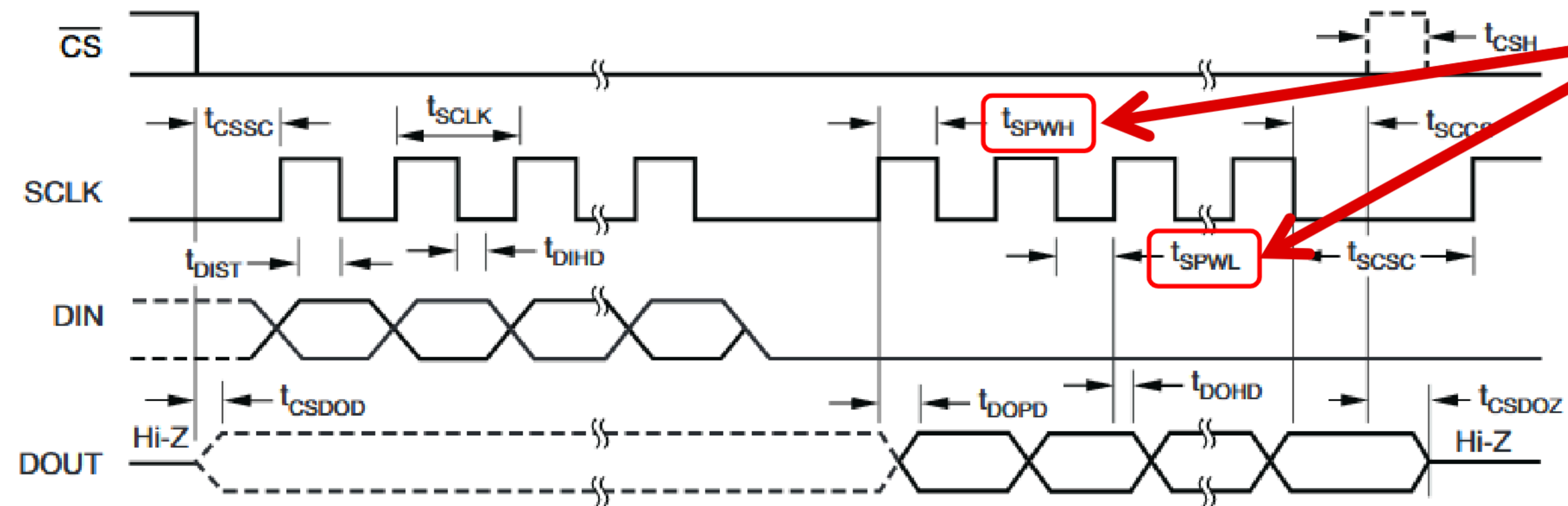


Figure 1. Serial Interface Timing

t_{SPWH} , t_{SPWL}

The minimum time for an SCLK high and the minimum time for an SCLK low

These two times with t_{SCLK} define how much skew in the SCLK duty cycle is allowed

For this device, there is a maximum t_{SPWL} for SPI timeout

SPI 时序图

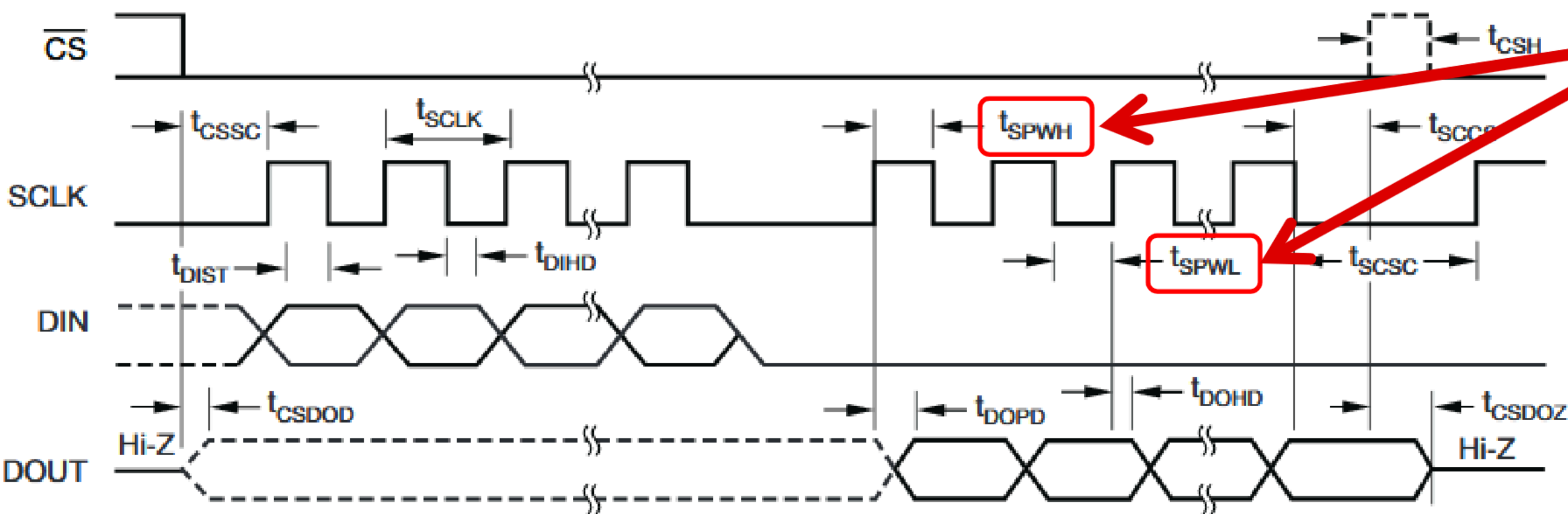


Figure 1. Serial Interface Timing

t_{SPWH} , t_{SPWL}

这定义了 SCLK 的最小时间，包括 SCLK 高电平的最小时间和 SCLK 低电平的最小时间。这两个时间与 t 共同决定了允许的 SCLK 占空比偏差。对于该设备，存在一个 SPI 超时的最大 t 值

SPI Timing Diagram

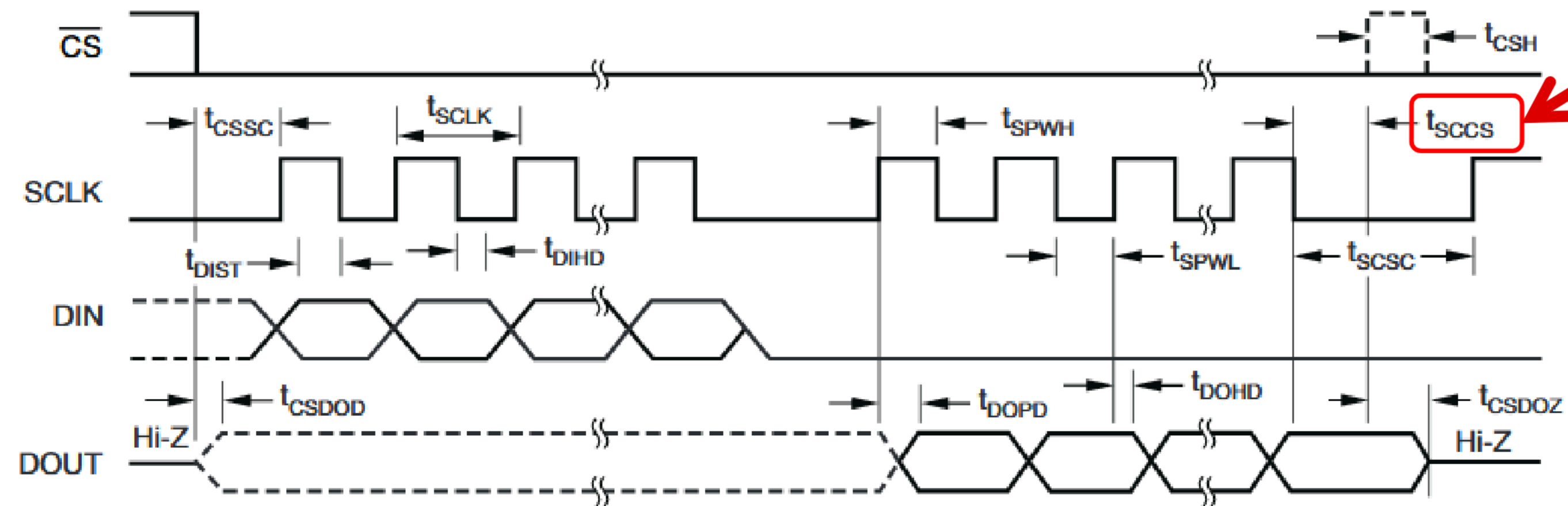


Figure 1. Serial Interface Timing

t_{SCSC}

Time from the falling edge of SCLK to the rising edge of CS

Because CS disables the SPI, ensure that the device receives the last bit of data before shutting down SPI communication

A violation of this could cause the device to miss the last data transmission

SPI 时序图

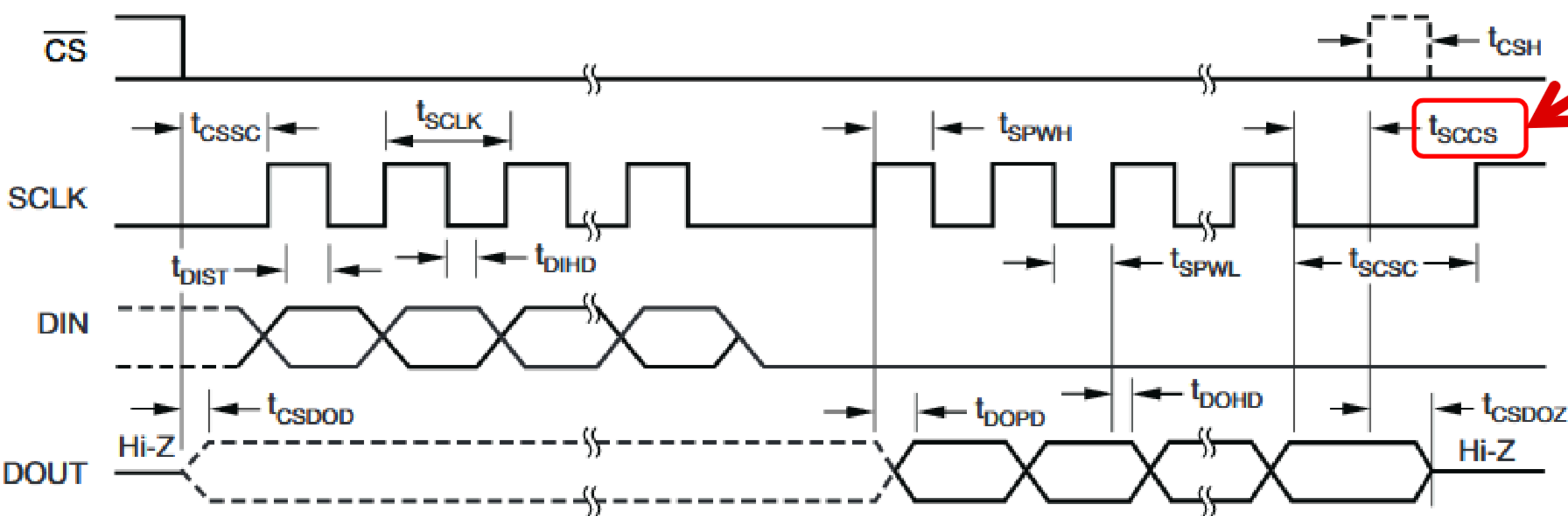


Figure 1. Serial Interface Timing

t_{SCCS}

从 SCLK 的下降沿到 CS 的上升沿的时间 因为 CS 禁用了 SPI，所以确保

设备在关闭 SPI 通信前接收最后一位数据。违反这一规定可能导致设备错过最后的数据传输

SPI Timing Diagram

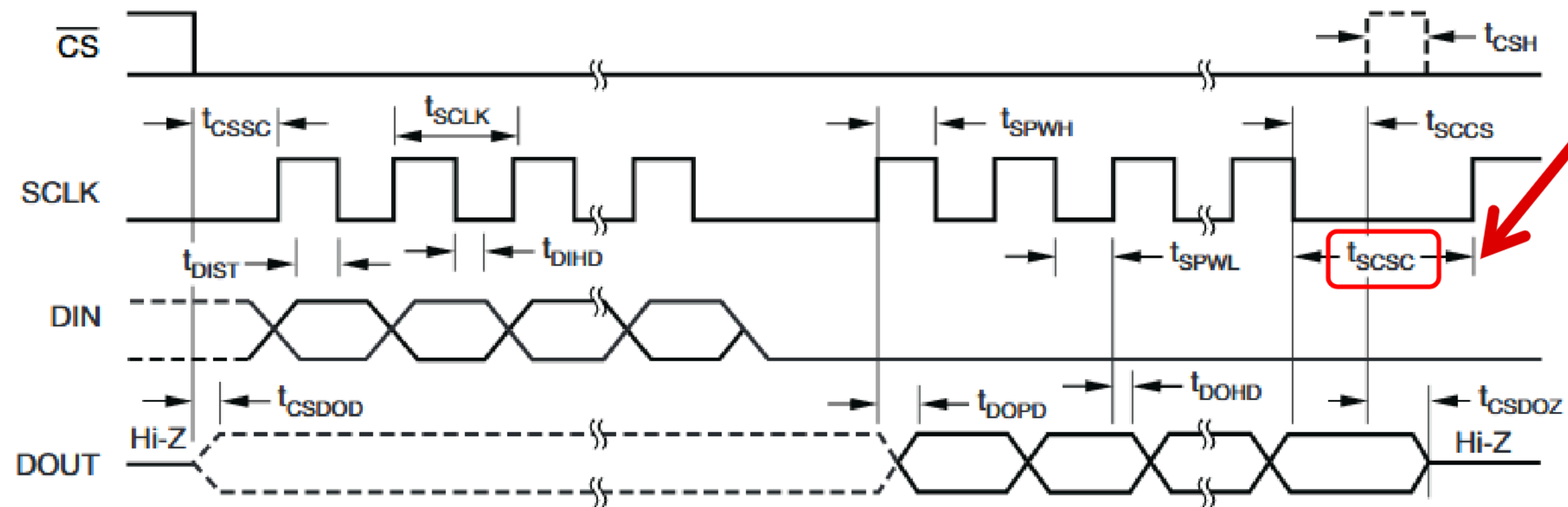


Figure 1. Serial Interface Timing

t_{SCSC}

Time from the falling edge of SCLK to the rising edge of SCLK in the next CS

This time is required to execute the command from one CS period, to start a new command in another CS period

SPI 时序图

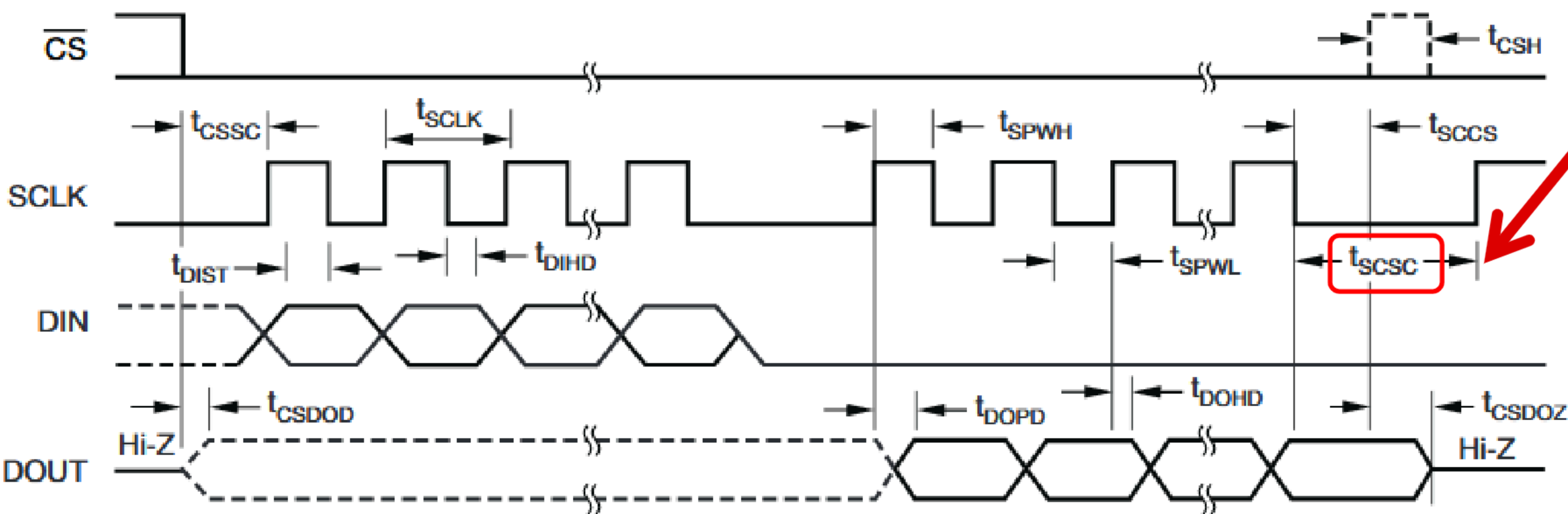


Figure 1. Serial Interface Timing

t_{SCSC}

从 SCLK 下降沿到下一个 CS 上升沿的时间

执行一个 CS 周期内的命令，并在另一个 CS 周期内开始新命令所需的时间

SPI Timing Diagram

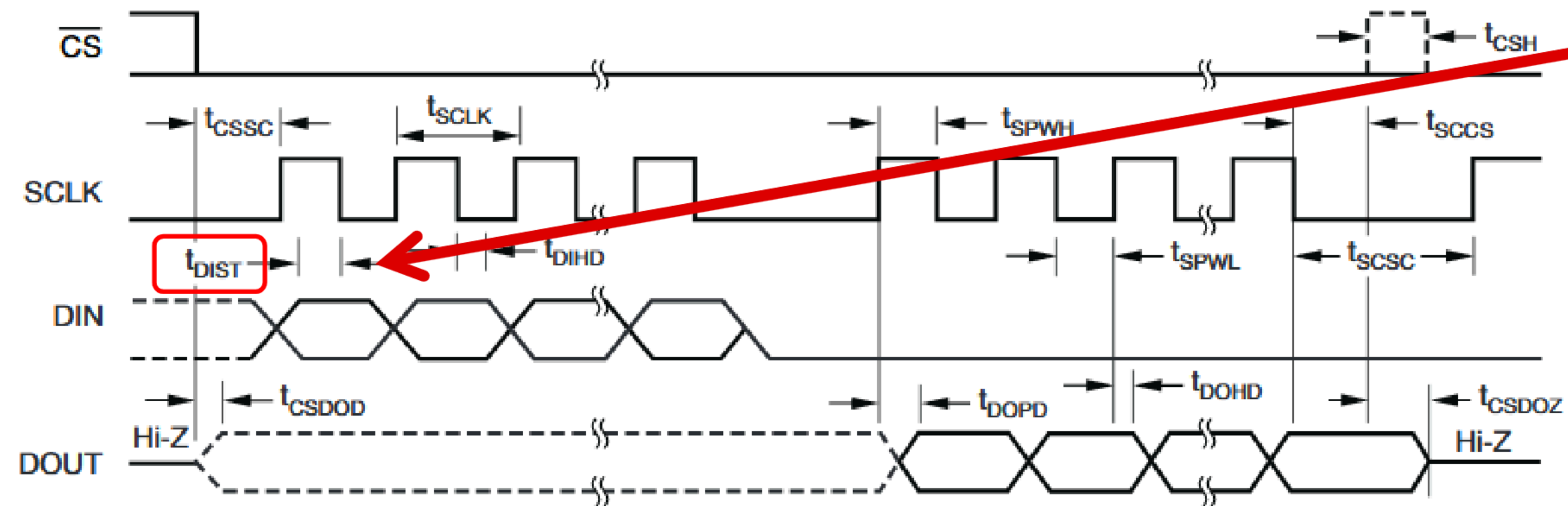


Figure 1. Serial Interface Timing

t_{DIST}

Setup time from the rising edge of DIN to the falling edge of SCLK

For data to be read into the device, the DIN must first be established for a time period before the SCLK falling edge.

SPI 时序图

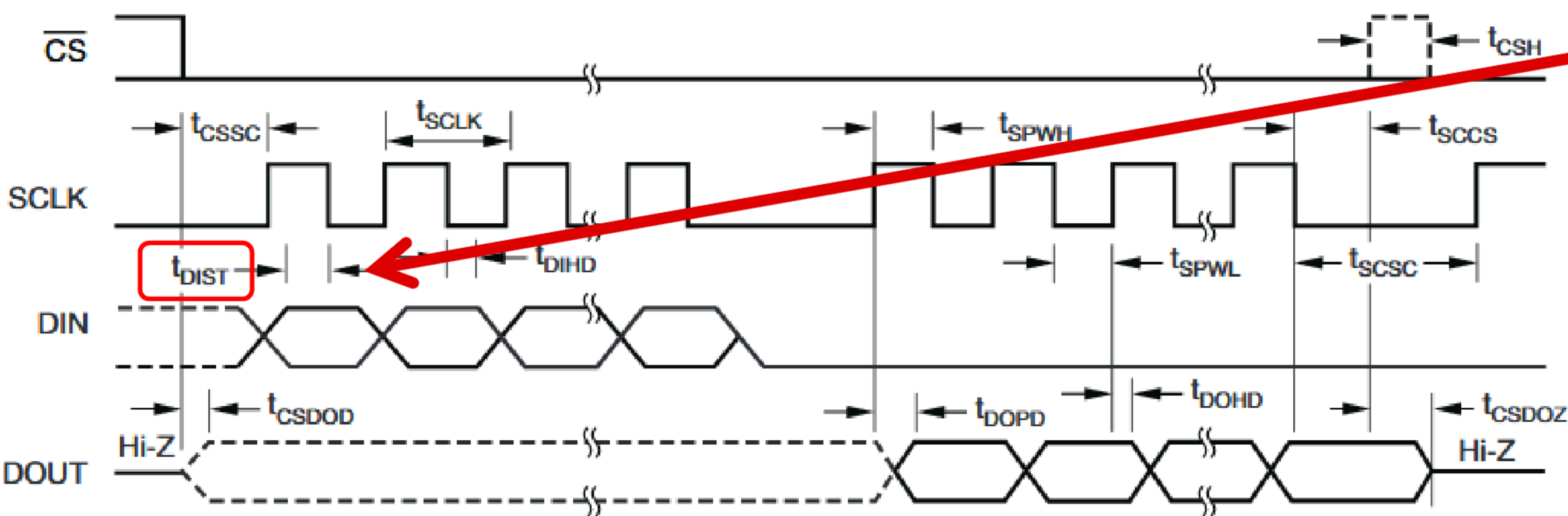


Figure 1. Serial Interface Timing

tDIST

从 DIN 的上升沿到 SCLK 的下降沿的建立时间 为了将数据读入设备，DIN 必须在 SCLK 下降沿之前建立一段时间。

SPI Timing Diagram

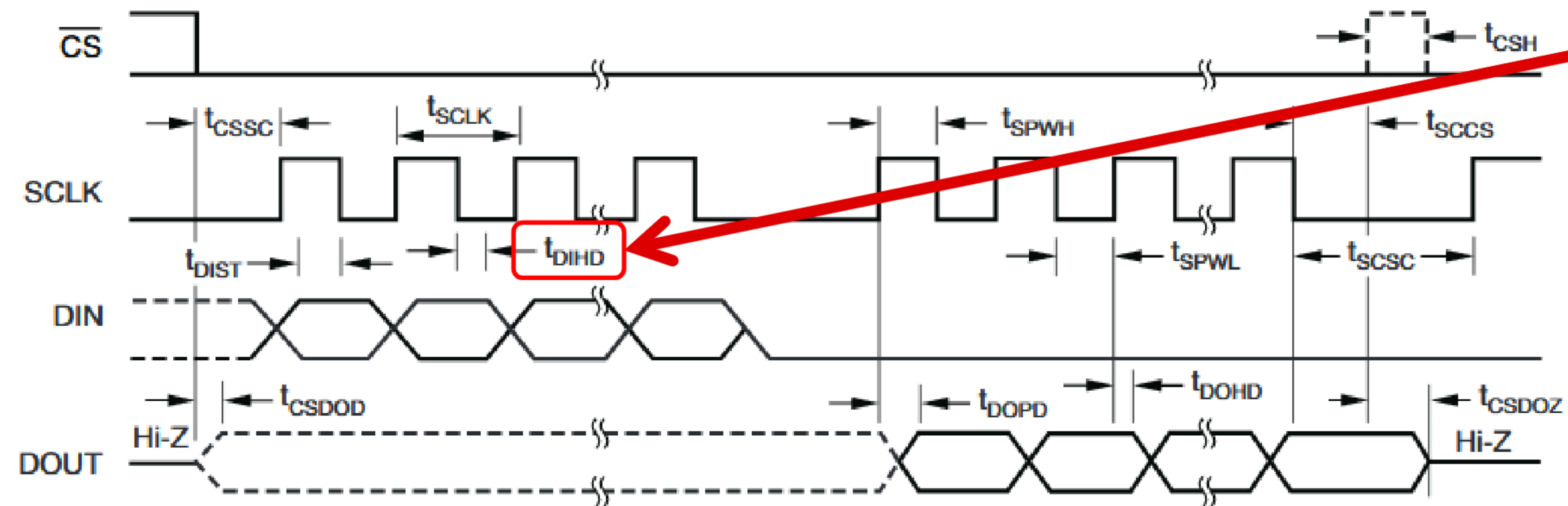


Figure 1. Serial Interface Timing

t_{DIHD}

Hold time from the falling edge of SCLK to the falling edge of DIN.

Once the data is set onto the DIN line, the SCLK falling edge latches the data into the device. However, there is a required time for the data to be held after the SCLK falling edge

SPI 时序图

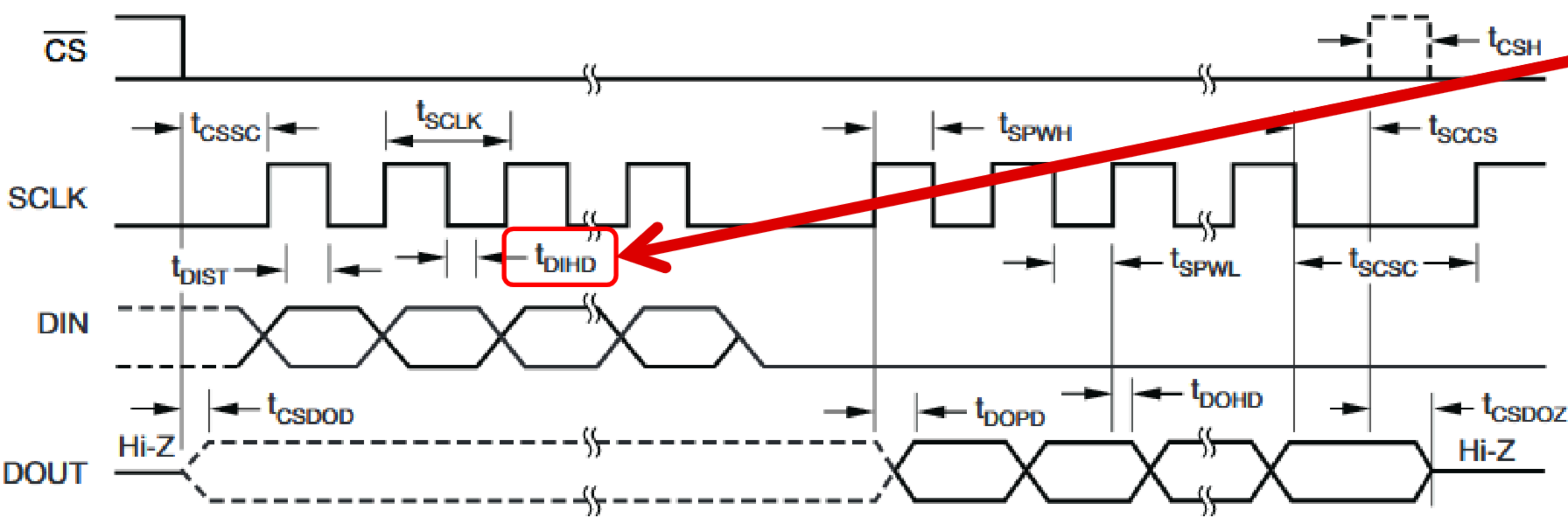


Figure 1. Serial Interface Timing

tDIHD

从 SCLK 的下降沿到 DIN 的下降沿的保持时间。一旦数据被设置到 DIN 线上，SCLK 的下降沿将数据锁存到设备中。然而，在 SCLK 下降沿之后，数据需要保持一段所需的时间

SPI Timing Diagram

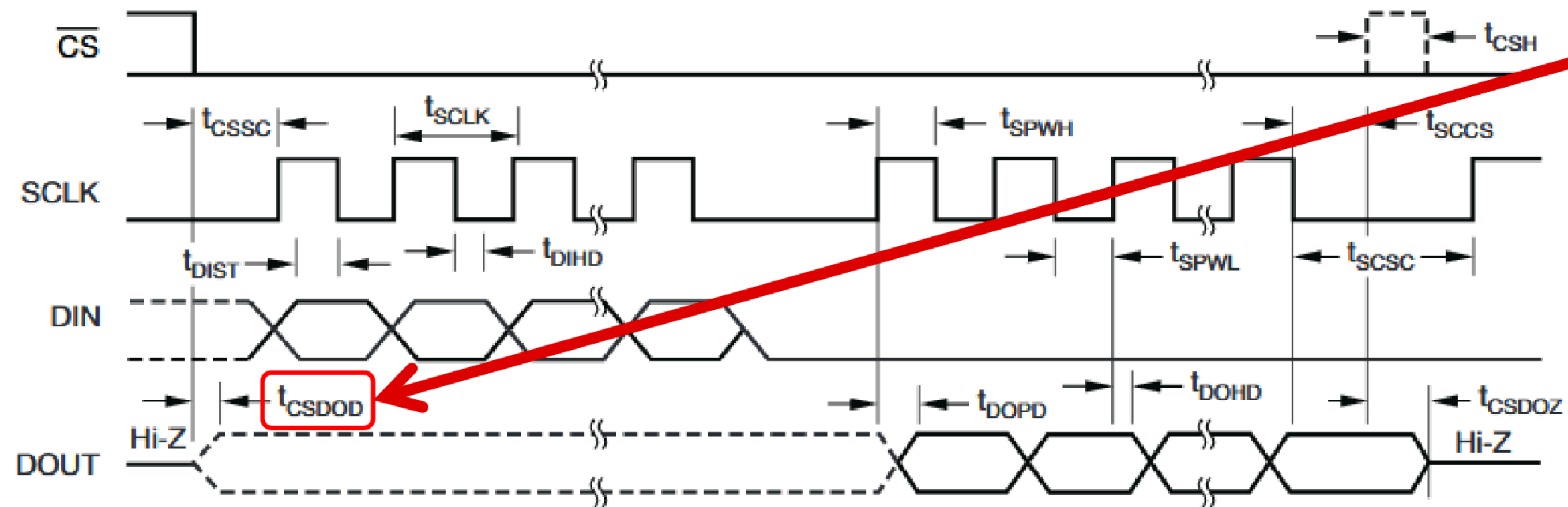


Figure 1. Serial Interface Timing

t_{CSDOD}

Propagation delay time from CS falling to DOUT actively driven

When CS is high, the DOUT is high impedance or Hi-Z, allowing for multiple devices on the bus to drive DOUT a device at a time.

When CS goes low, DOUT is actively driven

SPI 时序图

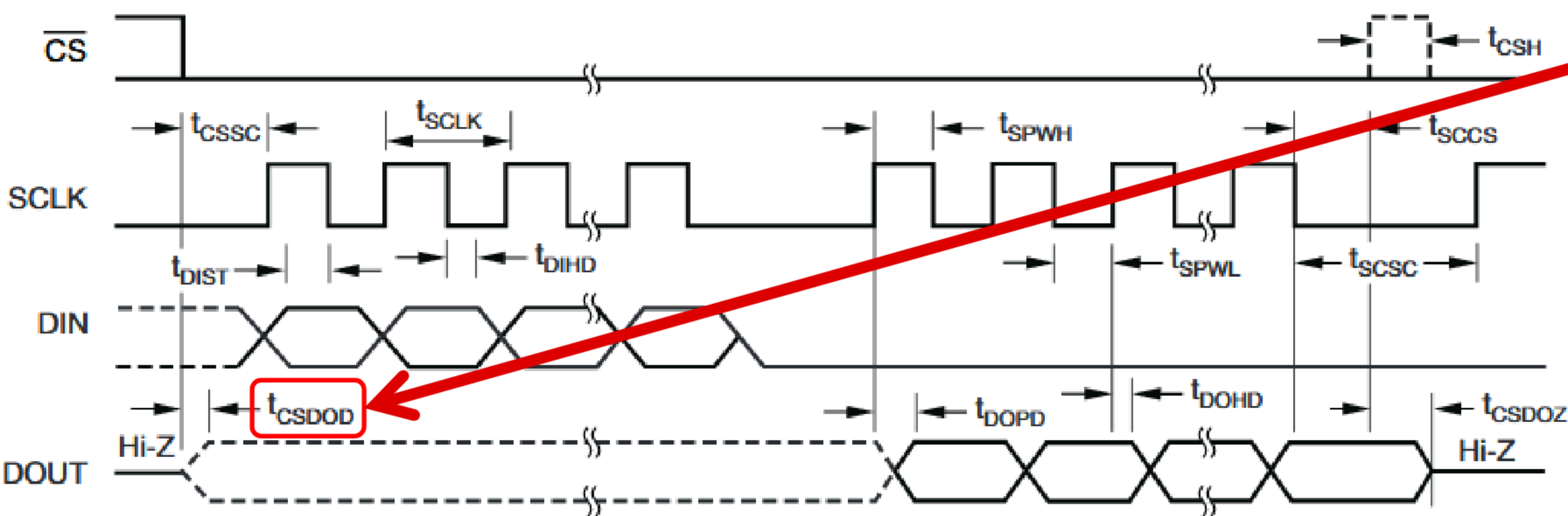


Figure 1. Serial Interface Timing

t_{CSDOD}

然而 CS 下降沿到 DOUT 主动驱动的传播延迟时间。当 CS 为高电平时，DOUT 呈高阻抗或 Hi-Z 状态，允许总线上多个设备逐个驱动 DOUT。当 CS 变为低电平时，DOUT 被主动驱动

SPI Timing Diagram

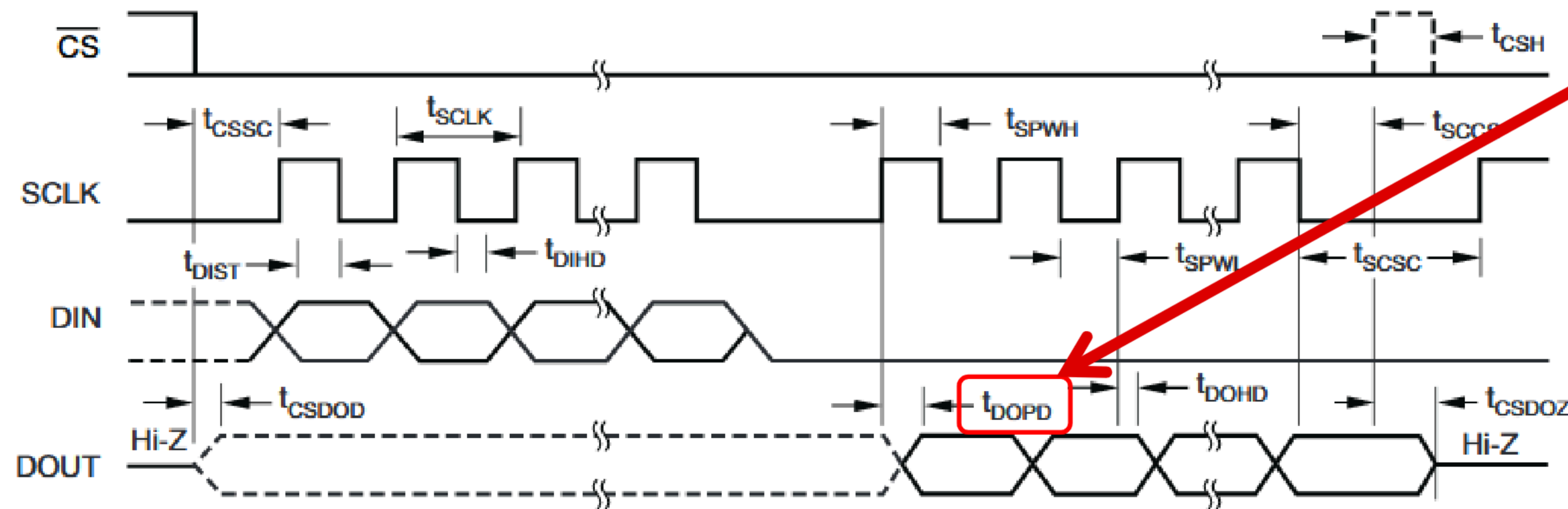


Figure 1. Serial Interface Timing

t_{DOPD}

Propagation delay time from rising edge of SCLK to data appearing on DOUT

SCLK is used to clock out data from the device. When SCLK is driven high, this signals to the device that data should be put on DOUT that can be clocked out on the falling edge of DOUT

SPI 时序图

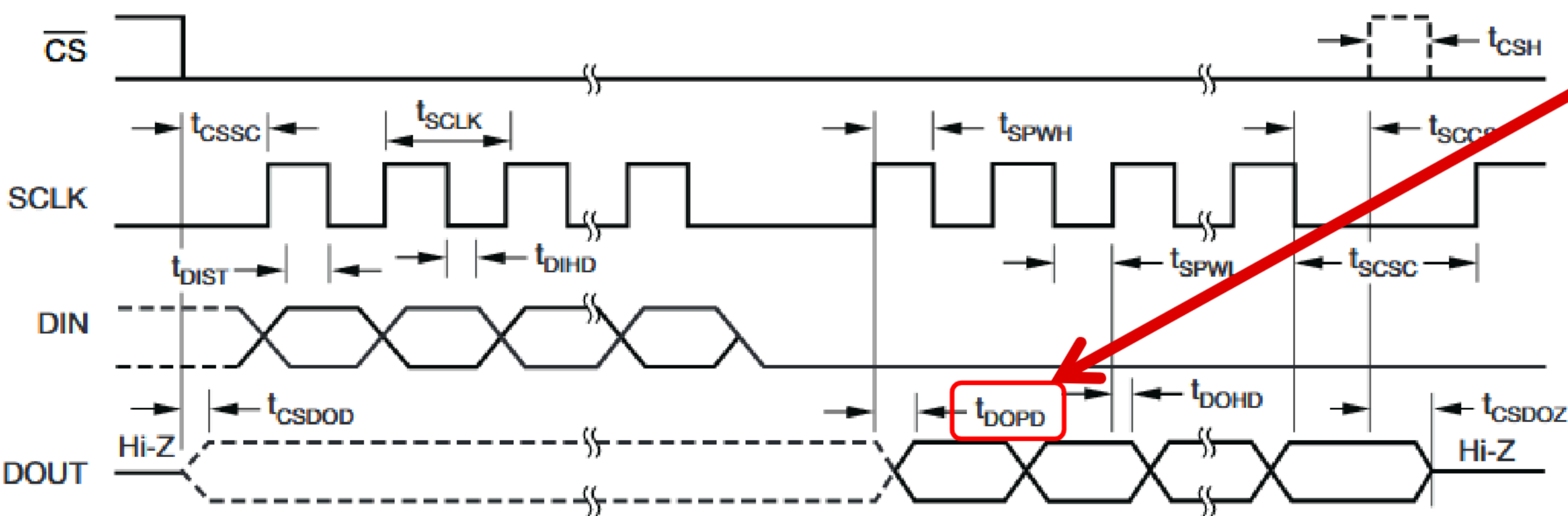


Figure 1. Serial Interface Timing

tDOPD

当 CS 变为低电平时，从 SCLK 的上升沿到 DOUT 上数据出现之间的传播延迟时间用于从设备中时钟输出数据。当 SCLK 被驱动为高电平时，这会向设备发出信号，表示数据应该放在 DOUT 上，该数据可以在 DOUT 的下降沿被时钟输出。

SPI Timing Diagram

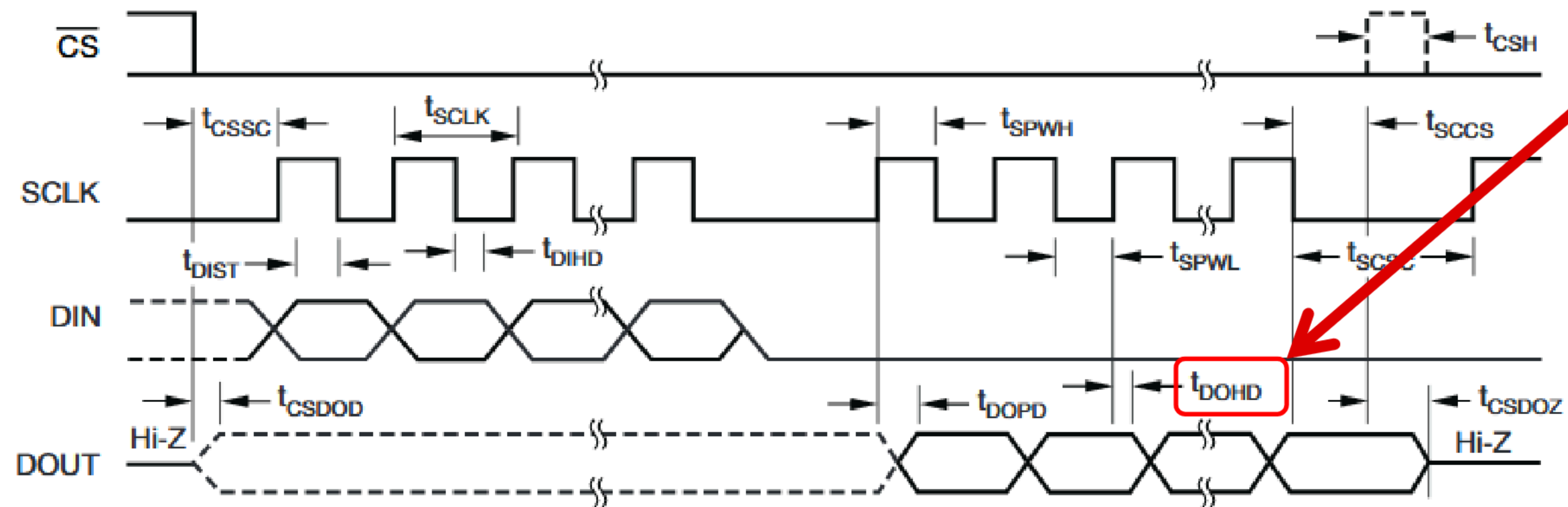


Figure 1. Serial Interface Timing

t_{DOHD}

Propagation delay time from rising edge of SCLK to data changing on DOUT

This defines the time for which the last data is still valid once the rising edge of SCLK occurs

SPI 时序图

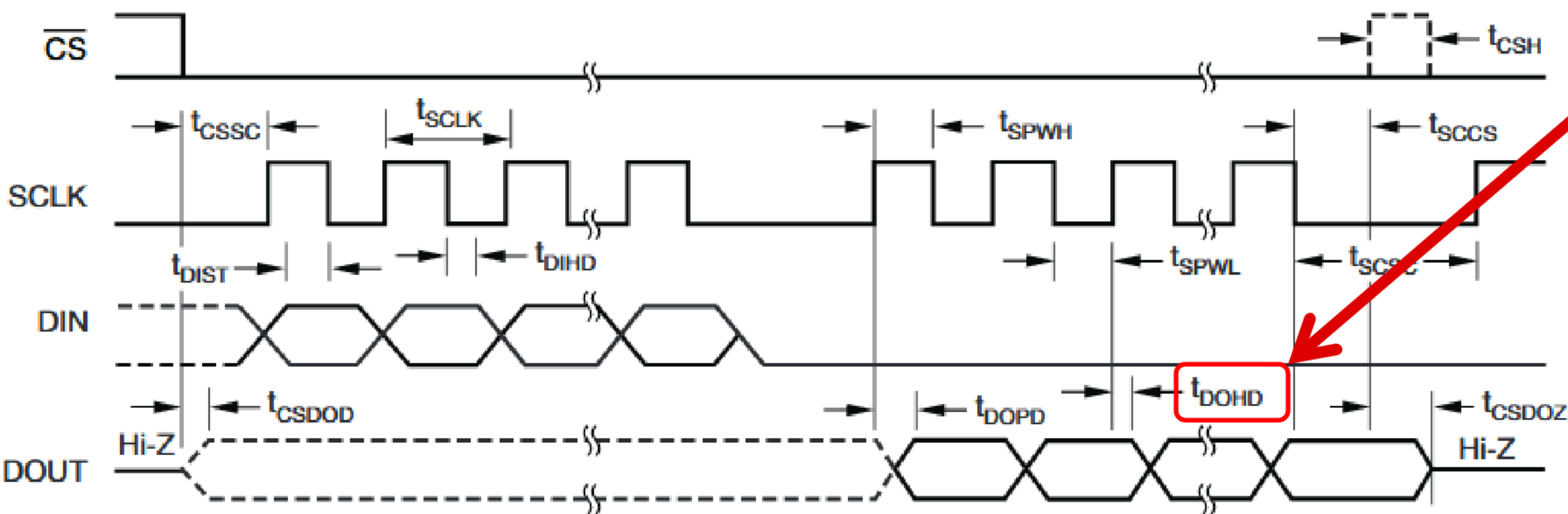


Figure 1. Serial Interface Timing

t_{DOHD}

当 SCLK 被驱动为高电平时，SCLK 上升沿到 DOUT 数据变化之间的传播延迟时间。这定义了 SCLK 上升沿发生后，最后数据仍然有效的持续时间

SPI Timing Diagram

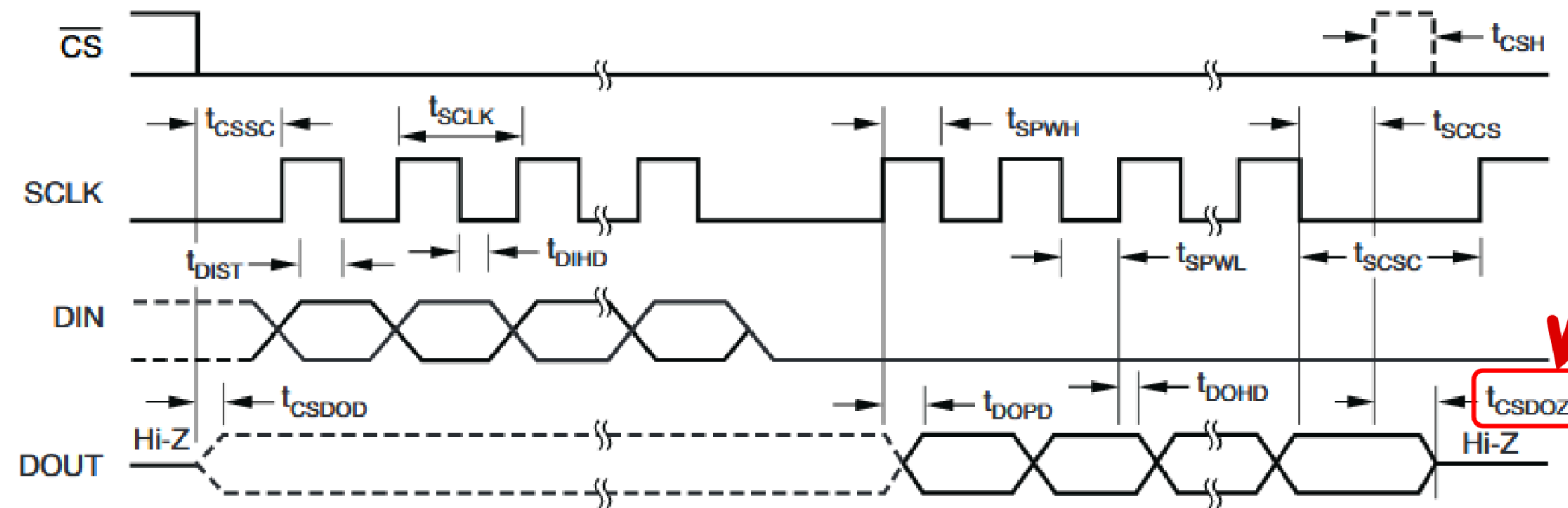


Figure 1. Serial Interface Timing

t_{CSDOZ}

Propagation delay time from rising edge of CS to DOUT becoming Hi-Z

SPI 时序图

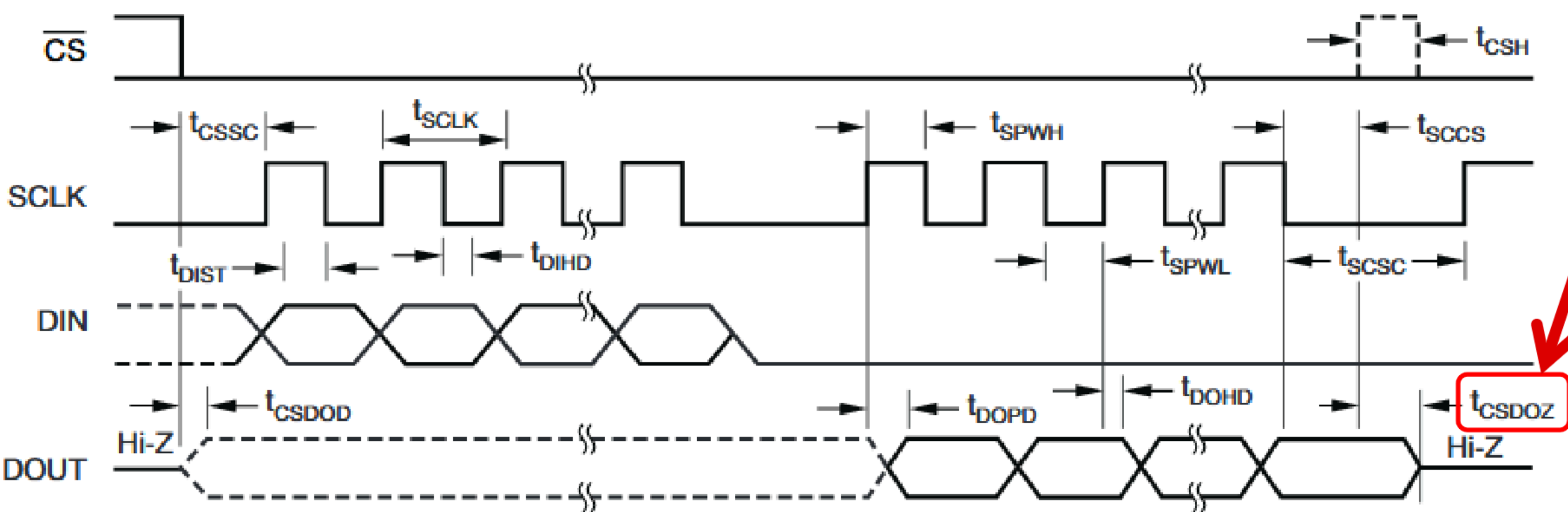


Figure 1. Serial Interface Timing

t_{CSDOZ}

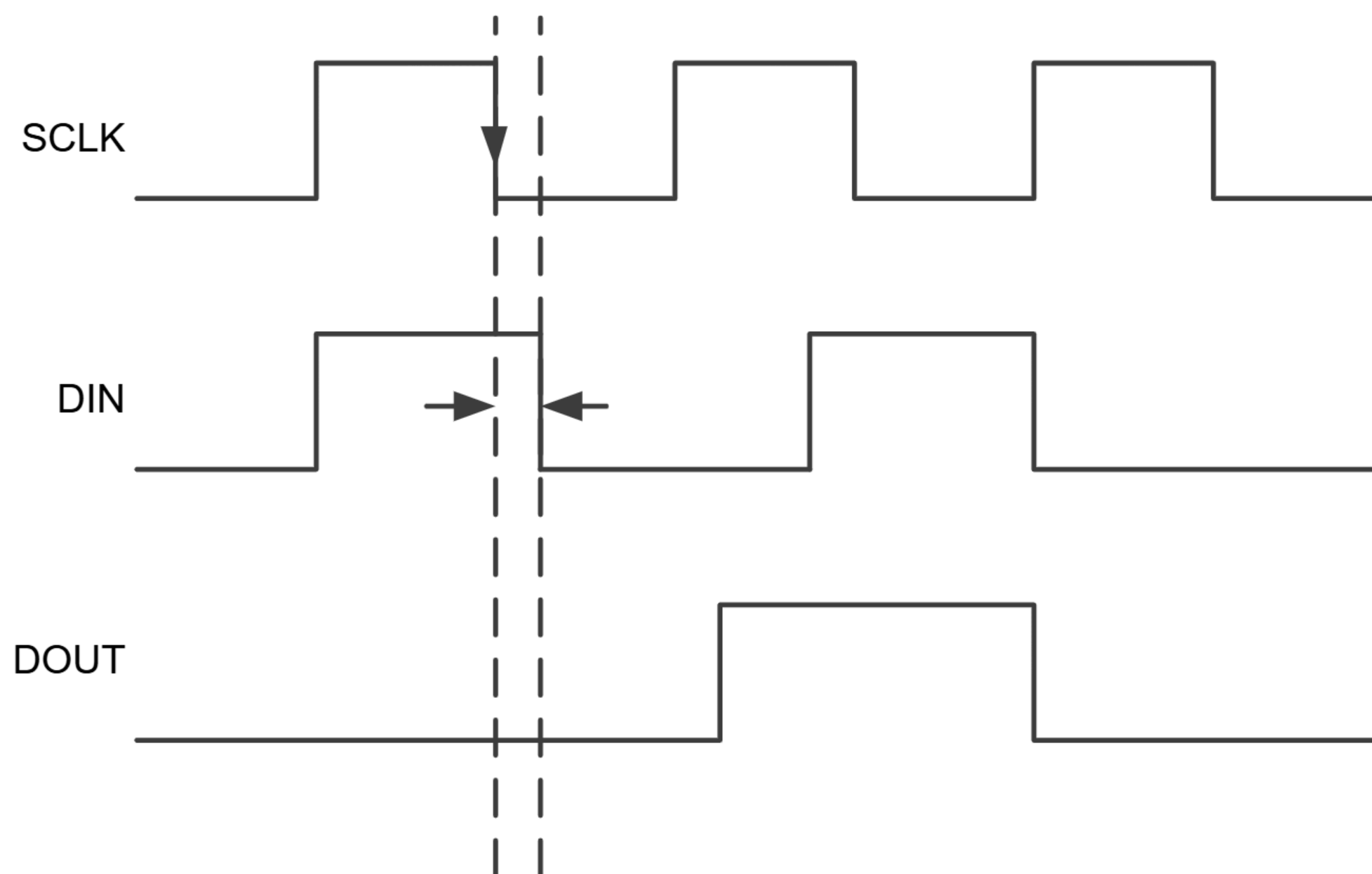
从 CS 上升沿到 DOUT 变为 Hi-Z 的传播延迟时间

Thanks for your time!
Please try the quiz.

感谢您的时间！ 请尝试测验。

Quiz: Basics of SPI: Timing Diagram

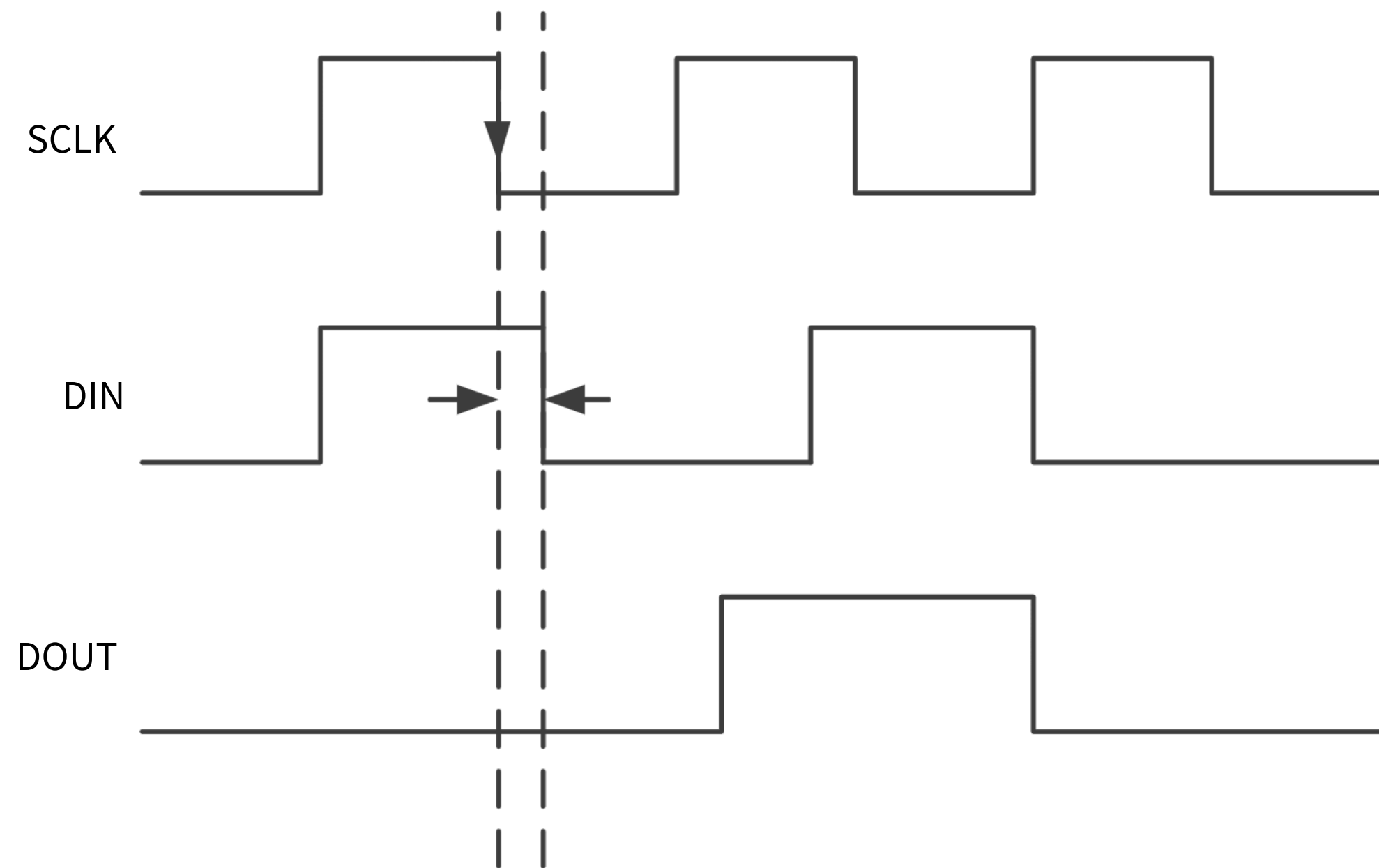
1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
- a. Setup time
 - b. Hold time
 - c. Propagation delay
 - d. None of the above



测验：SPI 基础：时序图

1. 如下图表为 $CPOL = 0$ ， $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿后保持稳定。这个时序是哪种时序要求的一个例子？

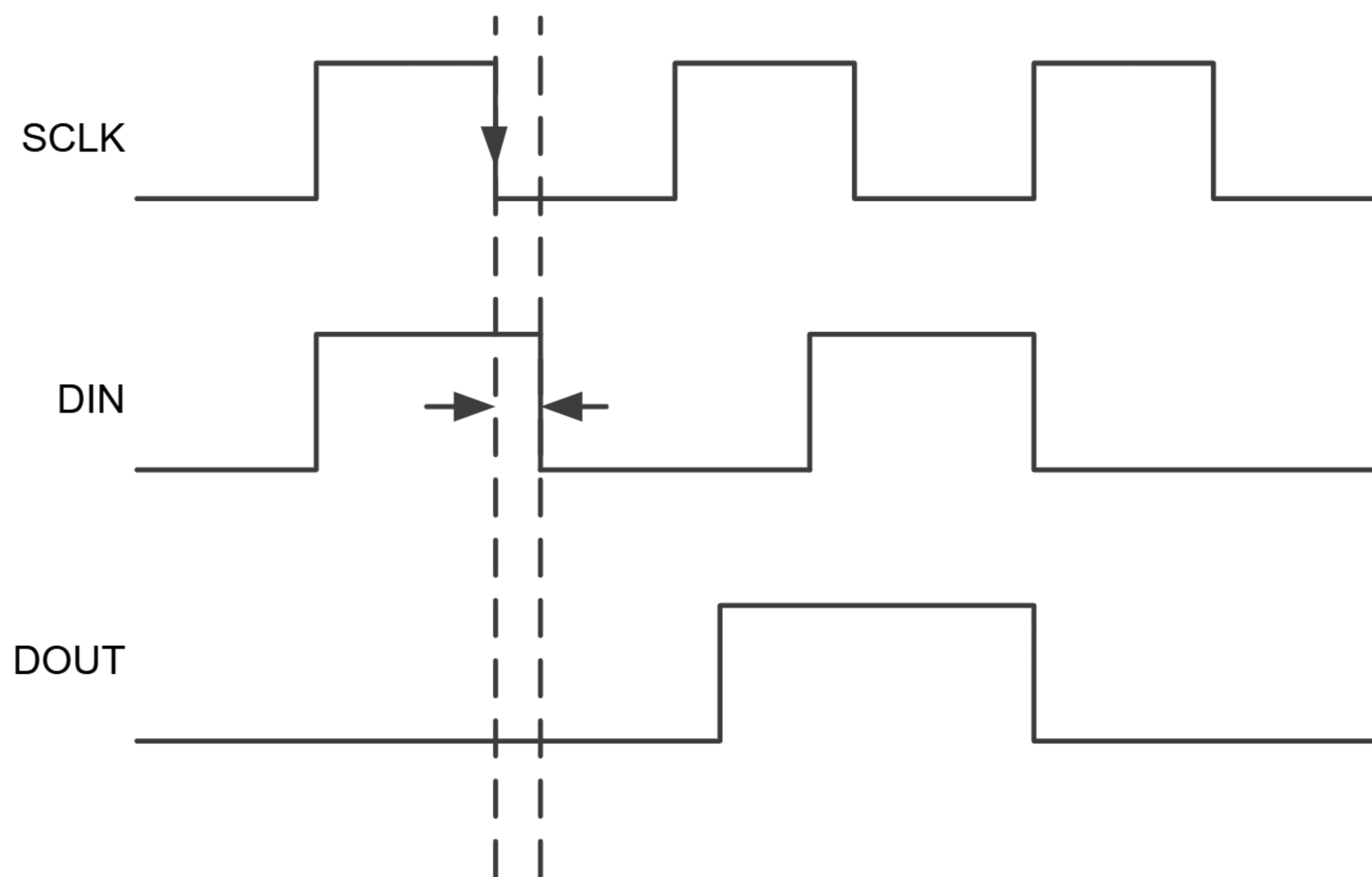
- a. 建立时间
- b. 持续时间
- c. 传播延迟
- d. 以上都不是



Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?

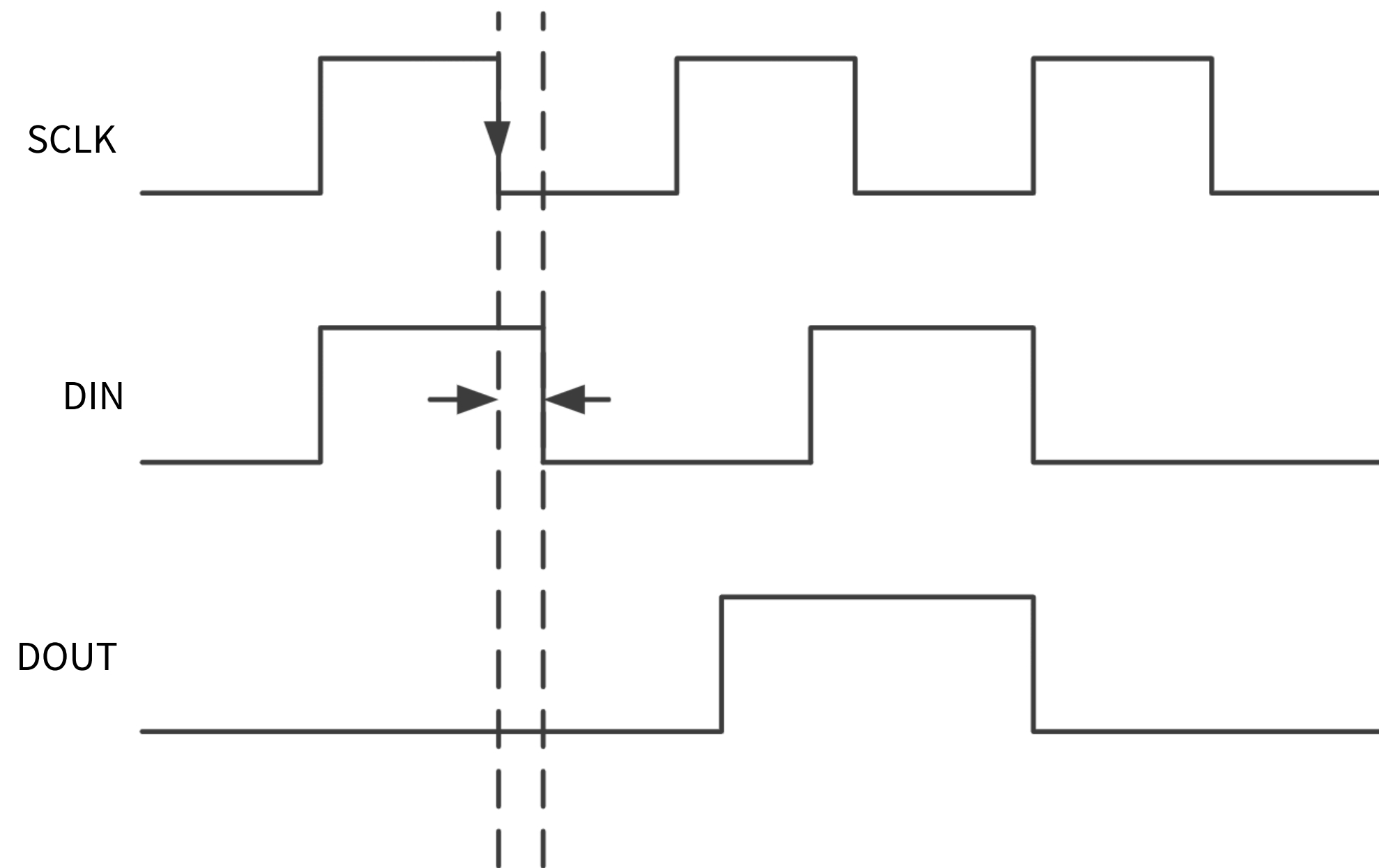
- a. Setup time
- b. Hold time**
- c. Propagation delay
- d. None of the above



测验：SPI 基础：时序图

1. 下面这个图是 $CPOL = 0, CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿之后保持稳定。这个时序是哪个时序要求的一个例子？

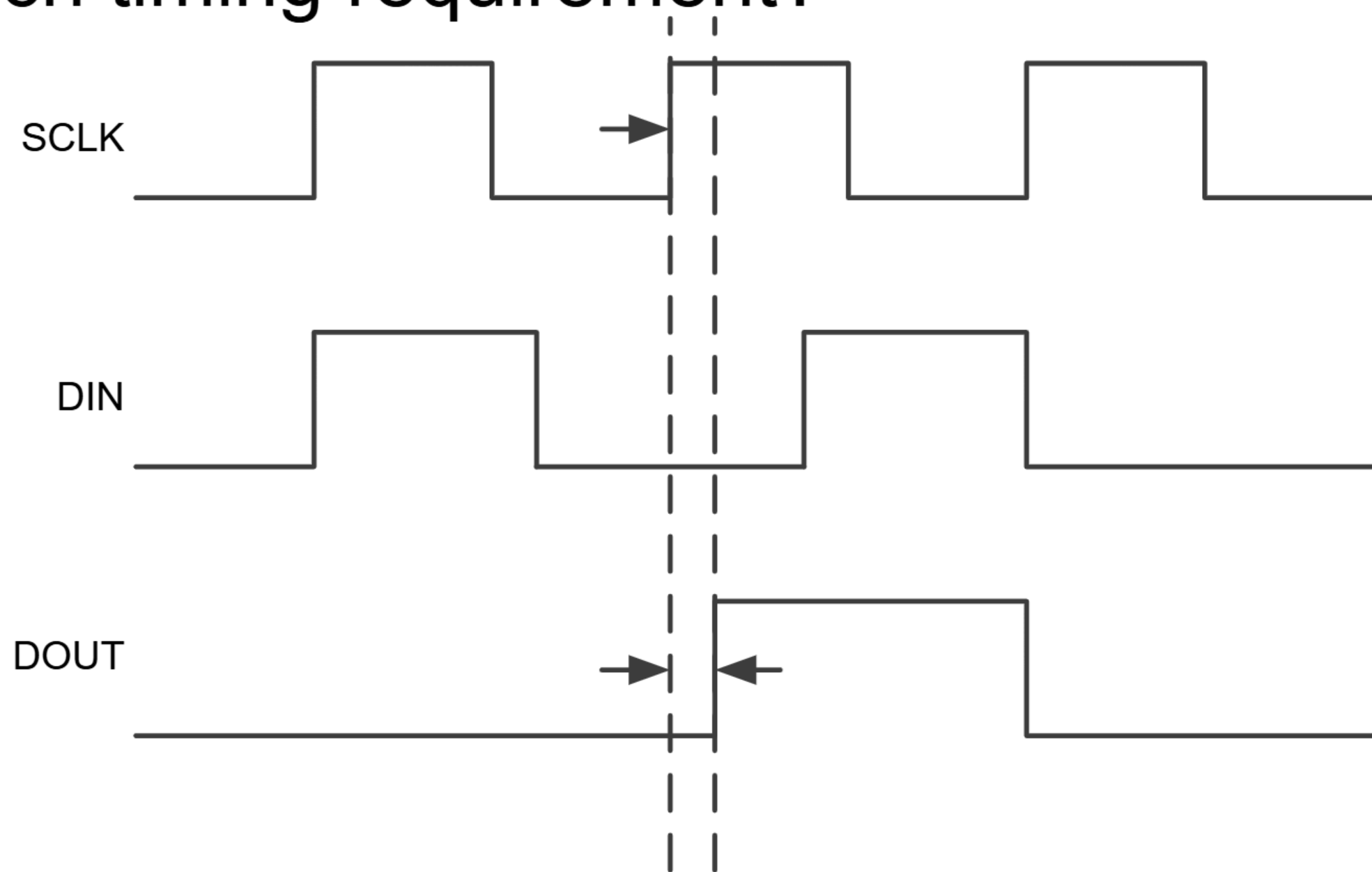
- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是



Quiz: Basics of SPI: Timing Diagram

2. The following diagram is $\text{CPOL} = 0$, $\text{CPHA} = 1$. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

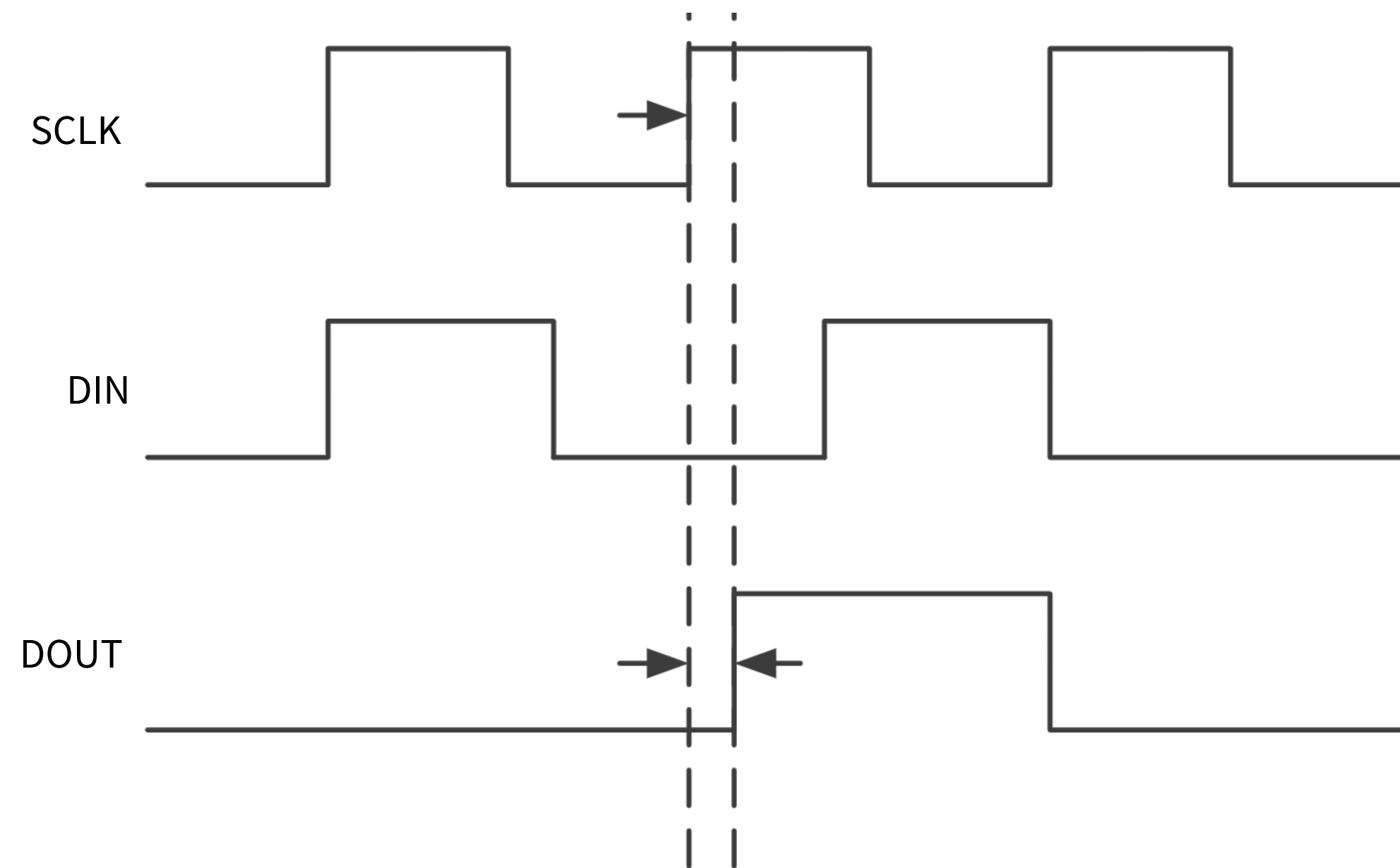
- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



测验：SPI 基础：时序图

2. 下列图表中 $CPOL = 0$ ， $CPHA = 1$ 。DIN 和 DOUT 在 SCLK 的下降沿读取。然而 DOUT 在 SCLK 的上升沿建立，并且数据到达 DOUT 可能需要时间。这种时序是哪种时序要求？

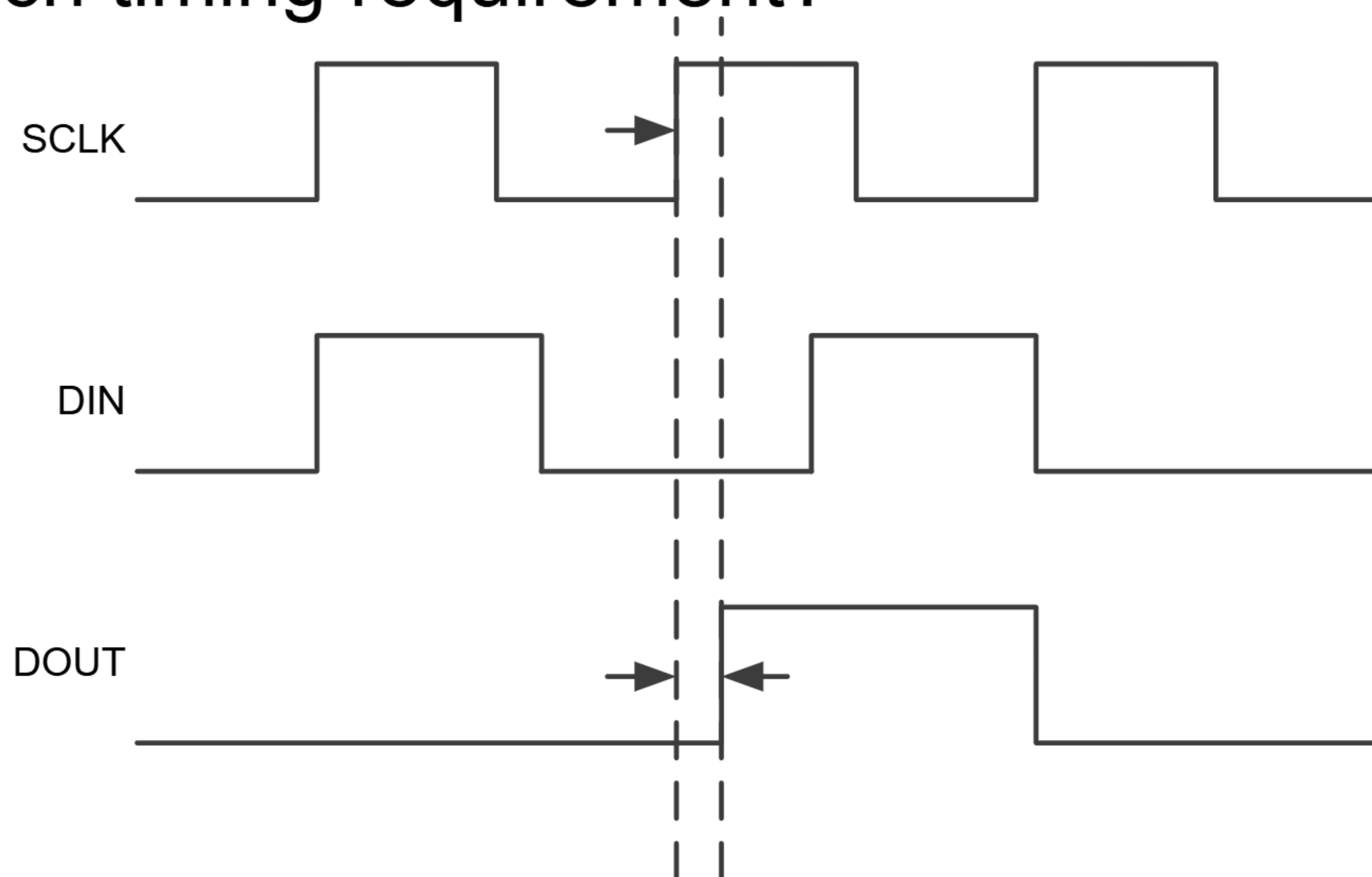
- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是



Quiz: Basics of SPI: Timing Diagram

2. The following diagram is $\text{CPOL} = 0$, $\text{CPHA} = 1$. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

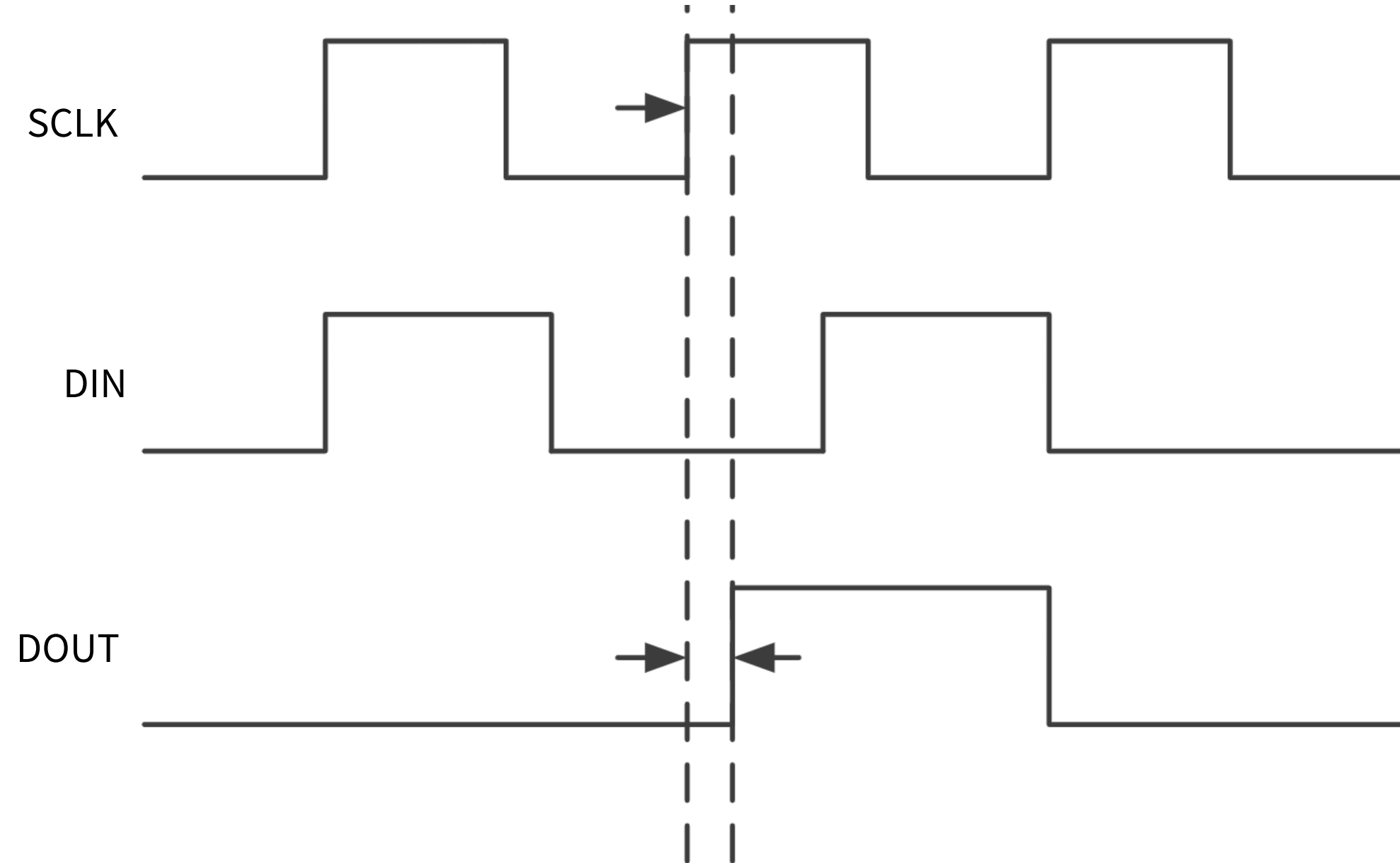
- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



测验：SPI 基础：时序图

2. 下列图表中 $CPOL = 0$, $CPHA = 1$ 。DIN 和 DOUT 在 SCLK 的下降沿读取。然而 DOUT 在 SCLK 的上升沿建立，并且数据到达 DOUT 可能需要时间。这种时序是哪种时序要求？

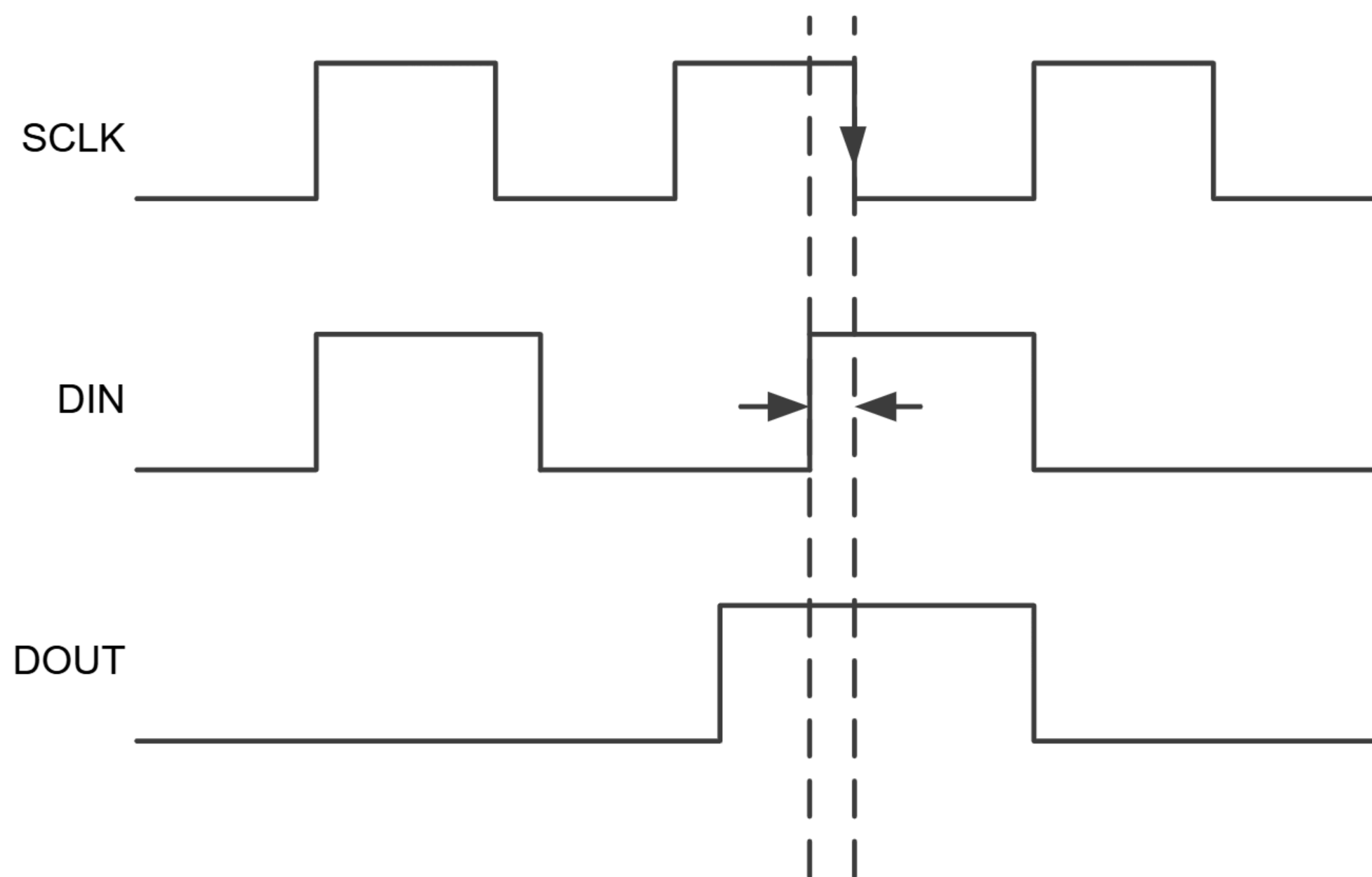
- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是



Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?

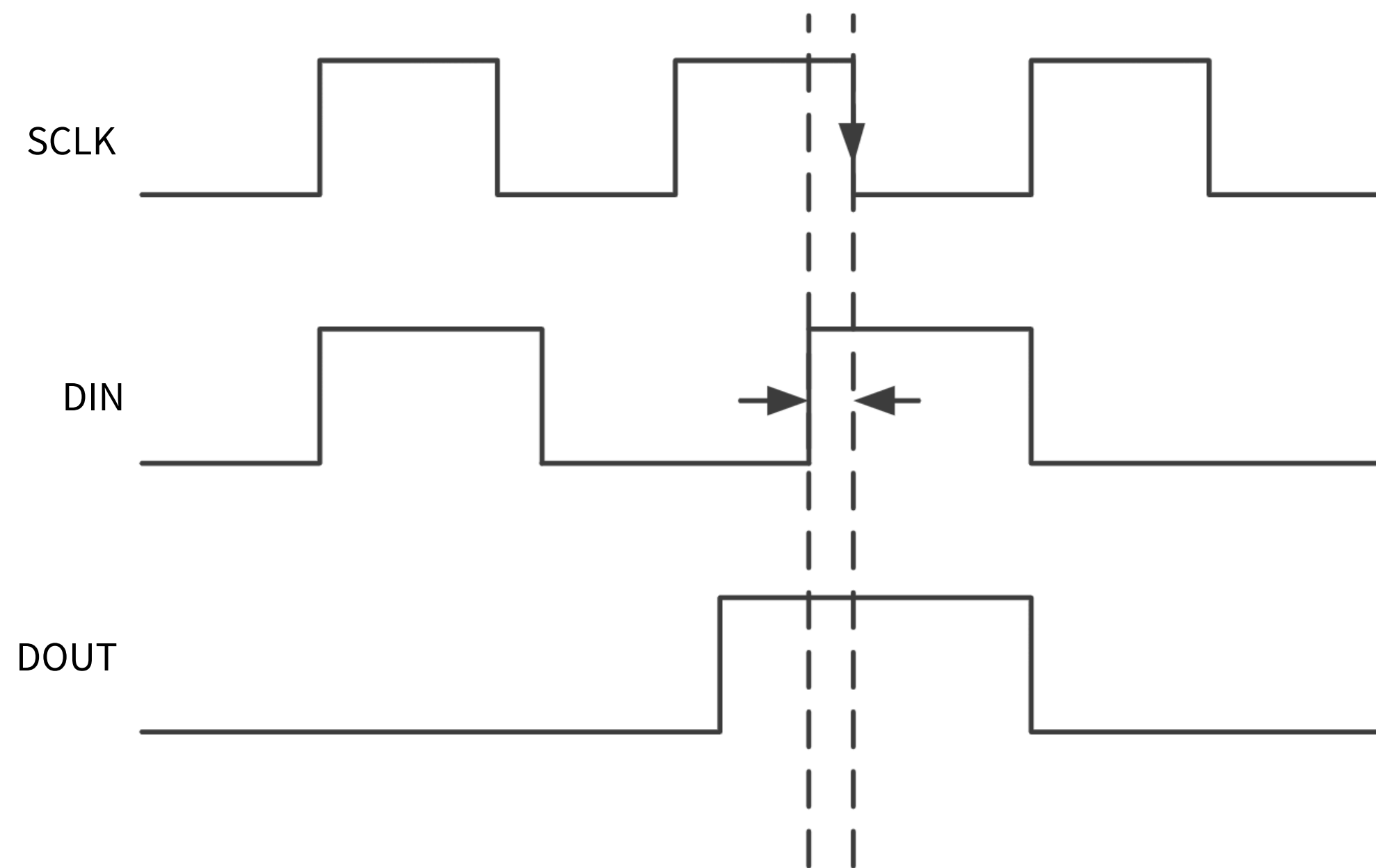
- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



测验：SPI 基础：时序图

3. 下图是 $CPOL = 0$ ， $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿之前保持稳定。这个时序是哪个时序要求的一个例子？

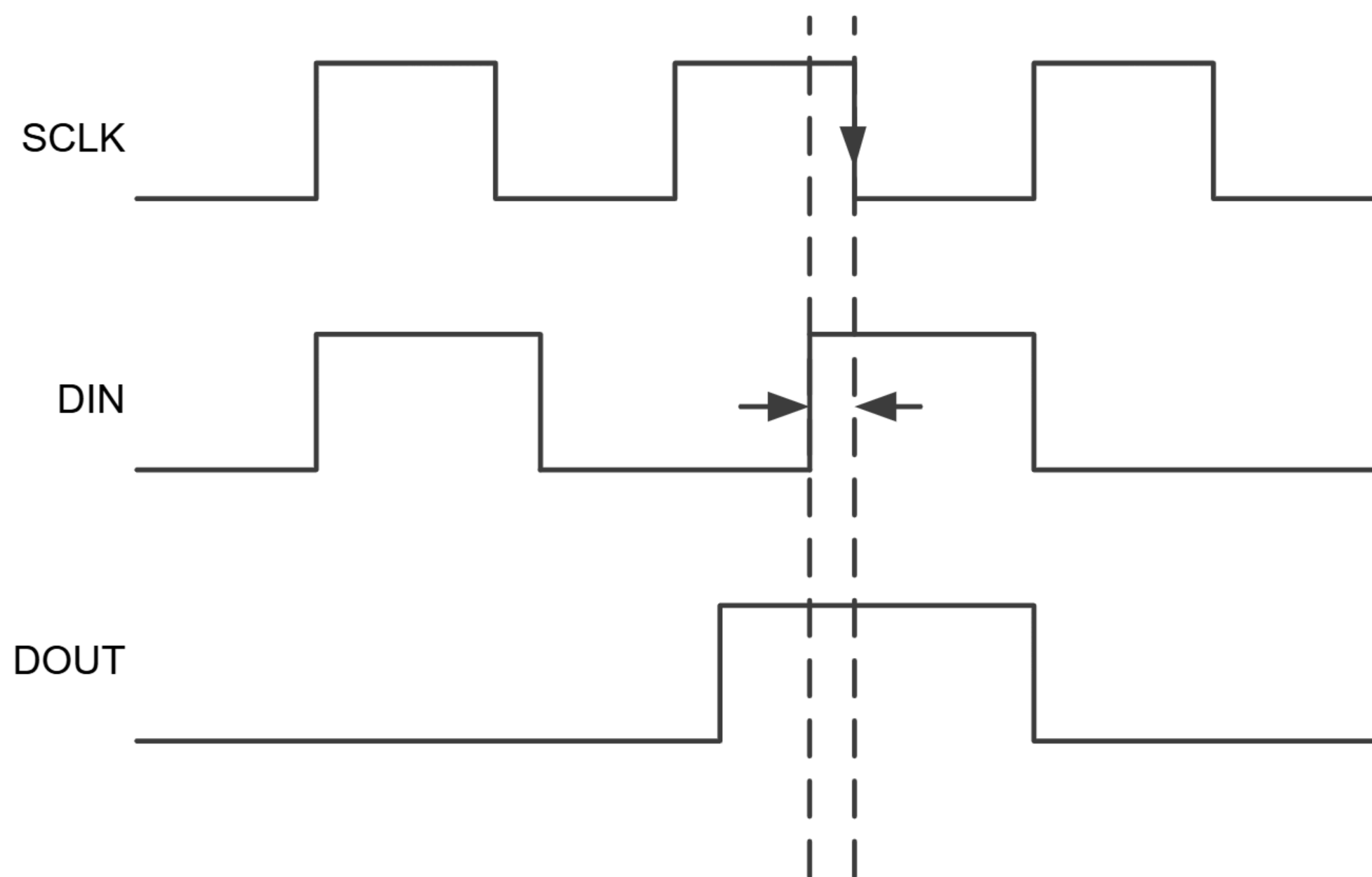
- a. 建立时间
- b. 持续时间
- c. 传播延迟
- d. 以上都不是



Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?

- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



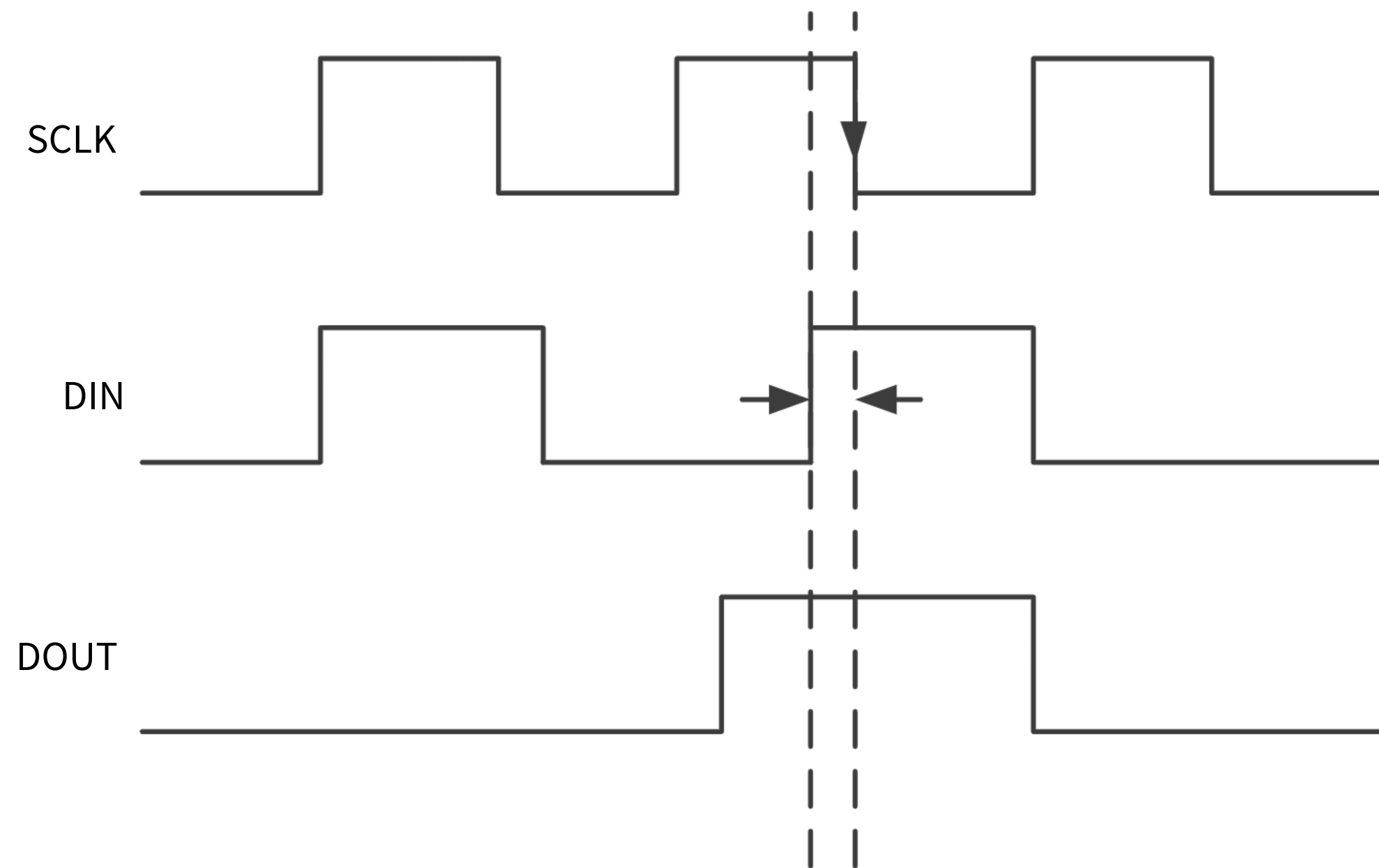
测验：SPI 基础：时序图

3. 下面的图示是 $CPOL = 0$, $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿之前保持稳定一段时间。这种时序是哪种时序要求的一个例子？

a. 建立时间

b. 持续时间 c. 传播延迟

d. 以上都不是



Thanks for your time!

感谢您的时间！



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Basics of SPI: Timing Requirements and Switching Characteristics

TIPL 6002

TI Precision Labs – Digital Communications

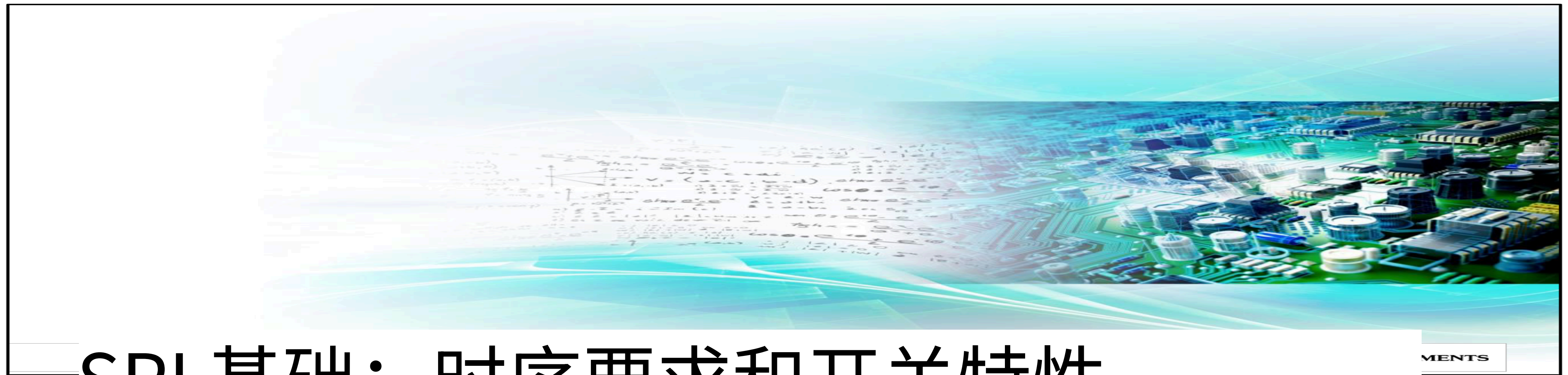
Presented by Alex Smith

Prepared by Joseph Wu



1

Hello, and welcome to our in-depth look at communications with precision data converters. In this video, we describe the timing requirements and switching characteristics between digital lines associated with Serial Peripheral Interface or SPI communication. We'll discuss timing and switching specifications that you may see in a datasheet. Then we'll describe an example of the timing diagram for one of TI's precision data converters.



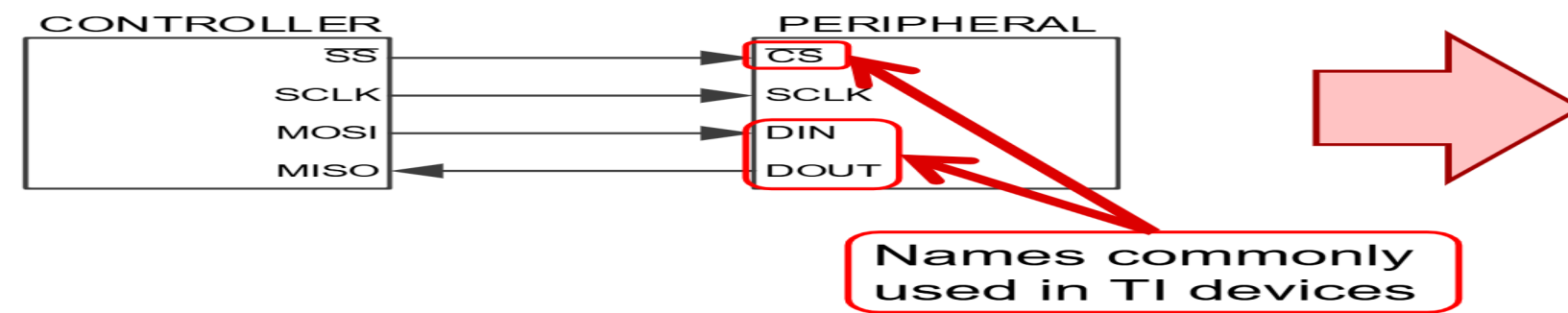
SPI 基础：时序要求和开关特性

TIPL 6002

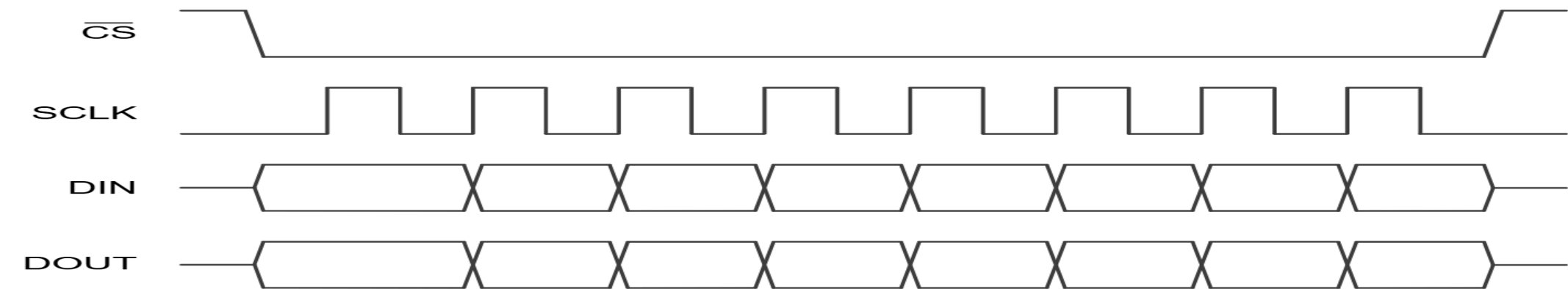
TI Precision Labs – 数字通信

由 Alex Smith 主讲，Joseph Wu 编写

SPI Communication



A timing diagram shows the specifications and the timing relationship between the SPI digital lines



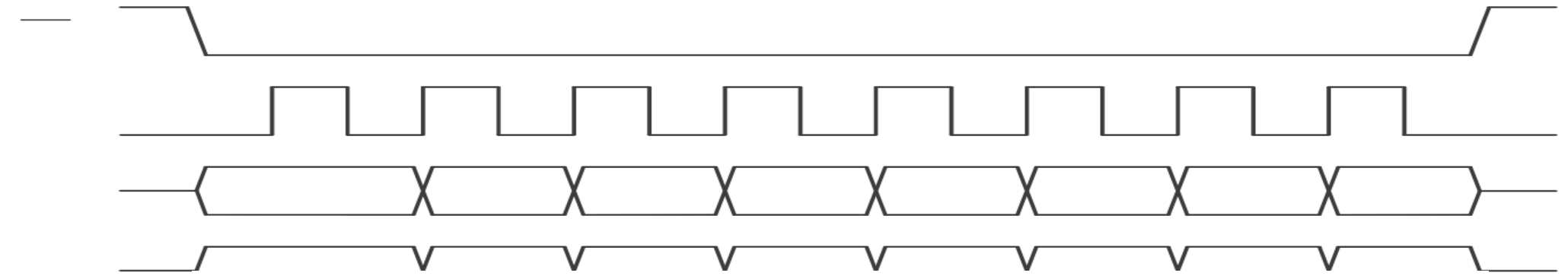
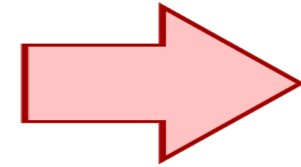
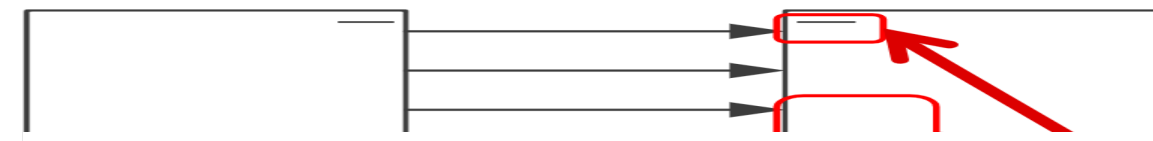
Violating a timing specification can cause a failure to read the data and may cause unexpected results.

In a previous video, we discussed how data is clocked into and out of precision data converters using the four digital lines of SPI. An active low peripheral select line, commonly known as Chip Select is used to select the device for communication. A serial clock of SCLK clocks data in and out of the peripheral device to the controller. Finally data lines of MOSI and MISO, commonly named DIN and DOUT for the peripheral device are used to send the data.

For all of these digital lines, there are specifications that define the time required from the change of one digital line to another. Many of these specifications are related to the time between the changes in the data of the DIN and DOUT lines to SCLK. These specifications ensure that the data is properly clocked into and out of the digital sections of the controller and peripheral device.

Regardless, all timing specifications must be followed to ensure that the controller and peripheral device are properly sending and receiving data. Violating a timing specification can cause failure to read the data and may cause unexpected results.

SPI 通信



时序图显示了 SPI 数字线之间的规范和时序关系

控制器外设

SS

CS

CS

SCLK

SCLK

MOSI

DIN

SCLK

MISO

DOUT

DIN

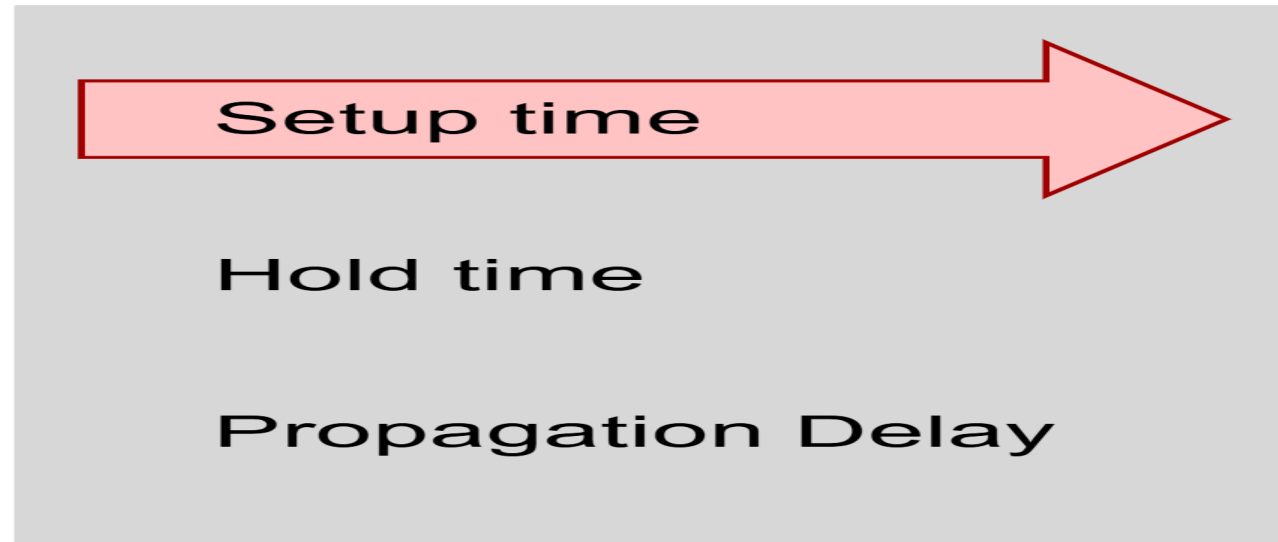
DOUT

名称通常
用于德州仪器设备

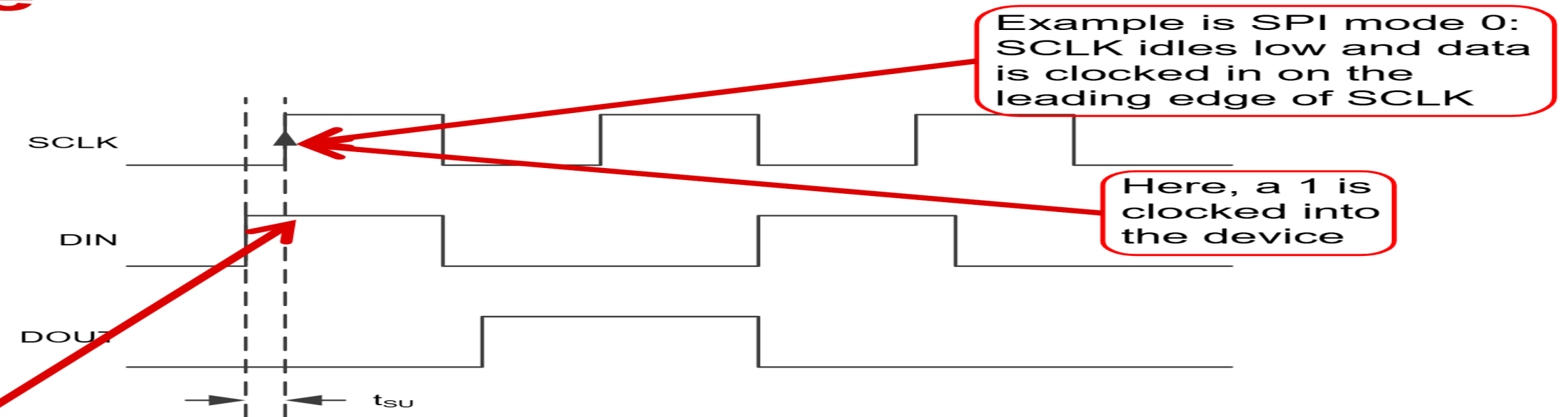


违反时序规范可能导致无法读取数据，并可能造成意外结果。

SPI Timing: Setup Time



The state of DIN is read into the device at the rising edge of SCLK. To ensure the data is correctly read, DIN must be at the correct state for a setup time **before** the SCLK rises



Setup time is the minimum time required before the clocking edge for which the data must be stable to be latched correctly

Most timing specifications can be categorized into one of three categories. They are setup times, hold times, or propagation delays. Using this timing diagram, we show the SCLK, DIN, and DOUT of a peripheral device. Using SPI mode 0, the SCLK idles low and the data is clocked in on the rising edge of the SCLK.

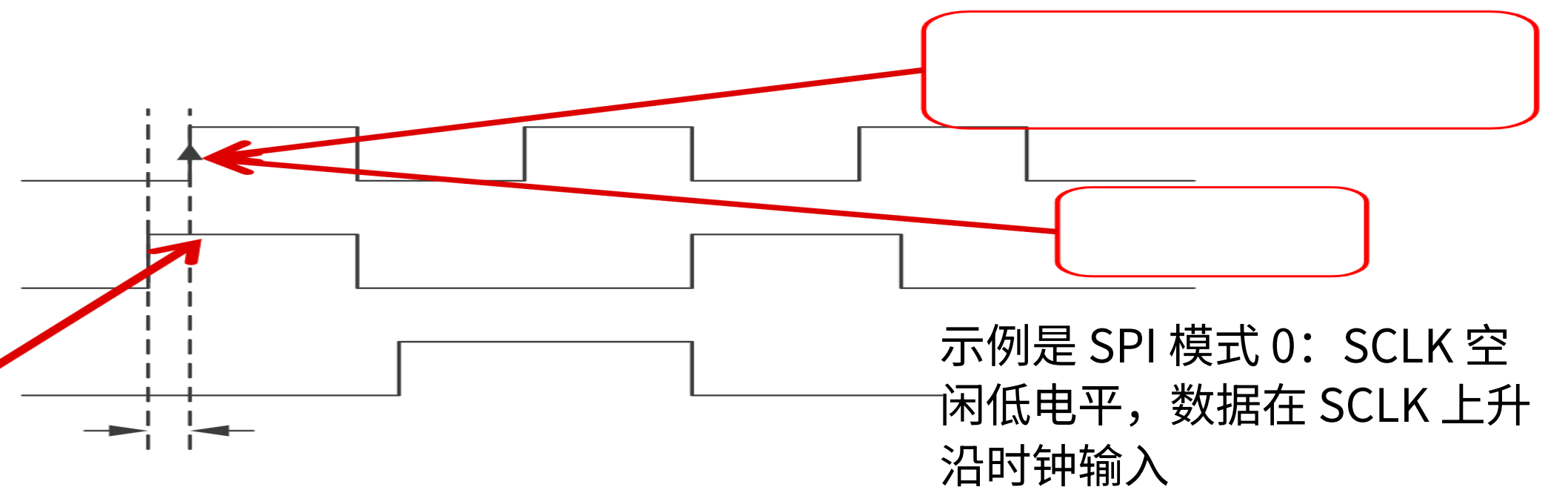
First, setup time is the time required for a data input to be stable *before* the edge of the clocking signal to be latched correctly. In the diagram, the example is SPI mode 0, where SCLK idles low and the data is clocked in on the rising edge of SCLK. DIN is set high so that at the rising edge of SCLK a 1 is clocked into the peripheral device. DIN must be set high first and it must stay high for a specific setup time so that the 1 is properly received.

SPI 时序：建立时间

建立时间

SCLK

TEXAS INSTRUMENTS



保持时间

DIN

在这里，一个 1 被
连接到
设备

传播延迟

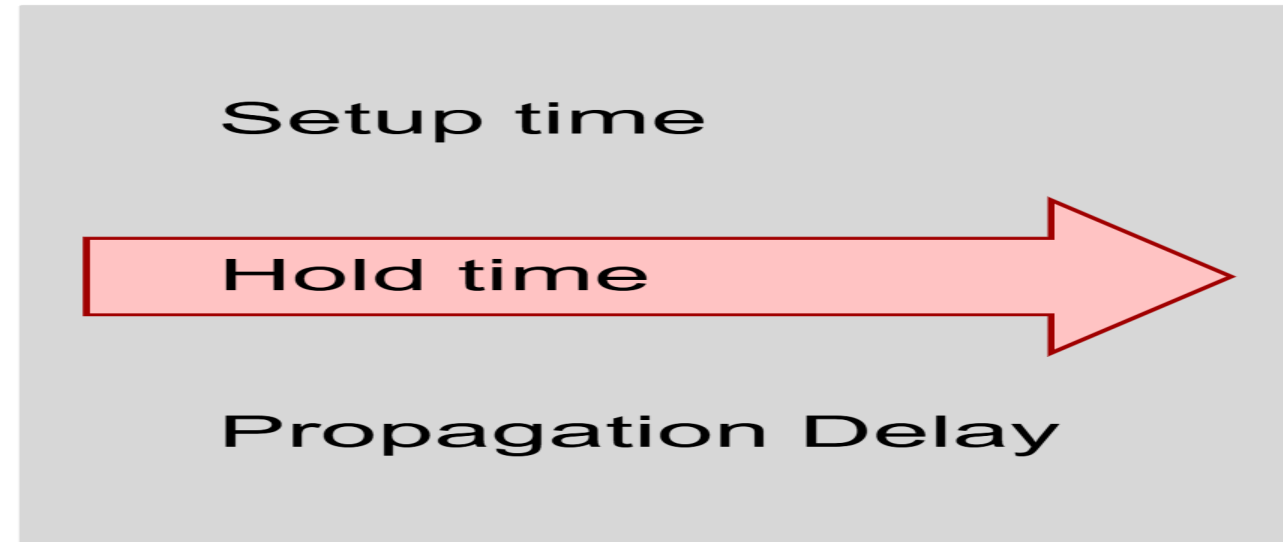
DOUT

t

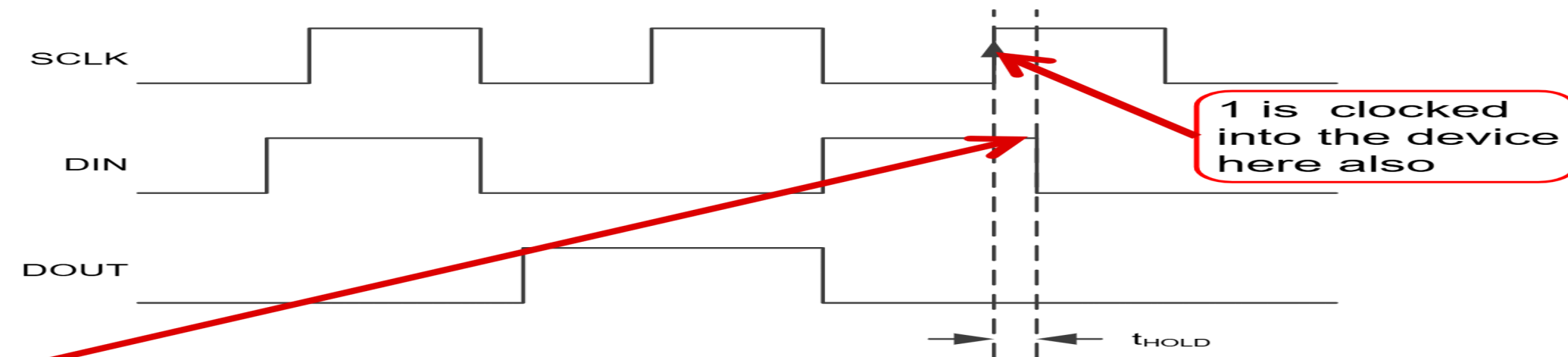
DIN 的状态在 SCLK 上升沿被读入设备。为确保数据正确读取，DIN 必须在 SCLK 上升前的建立时间内处于正确状态

建立时间是在时钟边沿之前必须保持稳定的最短时间，以确保数据能够正确锁存

SPI Timing: Hold Time



Again, the state of DIN is read into the device at the rising edge of SCLK. DIN must be held at the correct state for a hold time **after** the SCLK rises



Hold time is the minimum time required after the clocking edge for which the data must be stable to be latched correctly

Second, hold time is the time required for a data input to be held at the proper level *after* the clocking signal. In the diagram, DIN is already set high, and then the SCLK rises to clock in the signal. DIN must stay high for a hold time *after* the clock rises to ensure that the 1 again is properly received.

SPI 时序：保持时间

建立时间

SCLK



DIN

DOUT

t

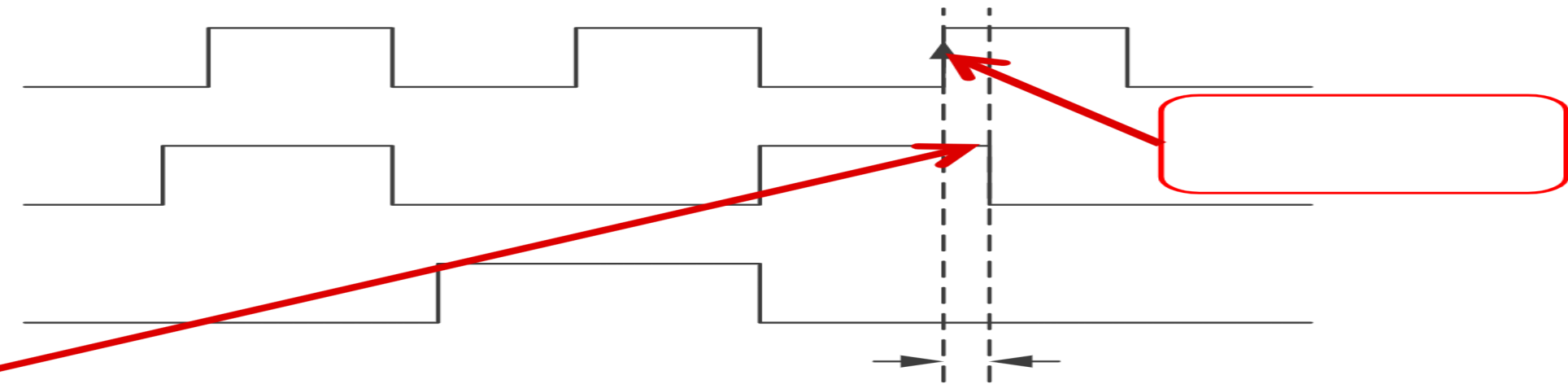
保持时间

传播延迟

1 被时钟同步
输入到设备
这里同样

同样，DIN 的状态在 SCLK 的上升沿被读入设备。DIN 必须在 SCLK 上升后保持正确状态一段时间

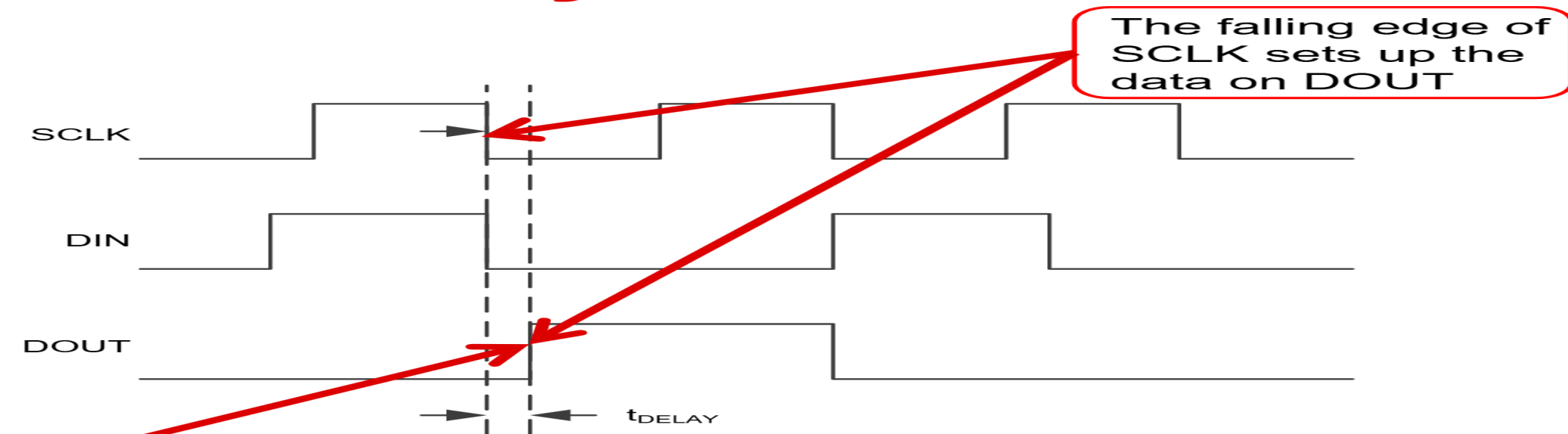
保持时间是指时钟边沿之后所需的最短时间，在此时间内数据必须保持稳定以确保正确锁存



SPI Switching: Propagation Delay



DOUT is read by the controller at the rising edge of SCLK. However, the peripheral sets the output at the previous falling edge of SCLK. This delay from one clock event to the response is a propagation delay.



Propagation delay is the time required for an input change to cause an output change through the digital circuitry

Lastly, there are propagation delays. This term describes the time required for the signal from one line to change the signal from another.

In the diagram, the SCLK comes into the device, and the controller reads DOUT on the rising edge of the clock. For the peripheral device, the falling edge of the clock sets up the next data bit so that by the rising edge of the clock when the controller reads the device, the correct data is on DOUT. This delay time describes how long it takes from the SCLK falling edge to place the data on the DOUT line.

SPI 切换：传播延迟

建立时间

SCLK

下降沿的
SCLK 设置
DOUT 数据

TEXAS INSTRUMENTS

保持时间

DIN

传播延迟

DOUT

t

DOUT 由控制器在 SCLK 的上升沿读取。然而，外设是在 SCLK 的前一个下降沿设置输出。从时钟事件到响应之间的这个延迟是传播延迟。

传播延迟是指输入变化导致数字电路输出变化所需的时间

SPI Timing

Timing Requirements
and Switching
Characteristics
example from the
ADS1118

7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

		MIN	MAX	UNIT
tCSSC	Delay time, CS falling edge to first SCLK rising edge ⁽¹⁾	100		ns
tSCCS	Delay time, final SCLK falling edge to CS rising edge	100		ns
tCSH	Pulse duration, CS high	200		ns
tSCLK	SCLK period	250		ns
tSPWH	Pulse duration, SCLK high	100		ns
tSPWL	Pulse duration, SCLK low ⁽²⁾	100		ns
tDIST	Setup time, DIN valid before SCLK falling edge	50	28	ns
tDIHD	Hold time, DIN valid after SCLK falling edge	50		ns
tDOHD	Hold time, SCLK rising edge to DOUT invalid	0		ns

(1) CS can be tied low permanently in case the serial bus is not shared with any other device.
(2) Holding SCLK low longer than 28 ns resets the SPI interface.

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tCSDOD	Propagation delay time, CS falling edge to DOUT driven			100	ns
tDOPD	Propagation delay time, SCLK rising edge to valid new DOUT	0		50	ns
tCSDOZ	Propagation delay time, CS rising edge to DOUT high impedance			100	ns

Timing Requirements
are typically setup
times and hold times

Switching Characteristics
are typically propagation
delays

Here we can take an in-depth look at SPI timing from an example datasheet. Using the ADS1118 precision ADC, two tables show the Timing Requirements and the Switching Characteristics. Typically, timing requirements show setup and hold times for the SPI communications and the switching characteristics will show propagation delays. These tables will give minimum and maximum times for different characteristics shown in a timing diagram.

SPI 时序

时序要求
和切换
特性
来自示例

ADS1118

7.6 Timing Requirements: Serial Interface

Over operating ambient temperature range and VDD = 2 V to 5.5 V (unless otherwise noted)

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tCSSC	Delay time, CS falling edge to first SCLK rising edge ⁽¹⁾	100		ns
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tDOHD	Hold time, SCLK rising edge to DOUT invalid			ns

1) CS can be tied low permanently in case the serial bus is not shared with any other device.
2) Holding SCLK low longer than 28 ms resets the SPI interface.

7.7 Switching Characteristics: Serial Interface

Over operating ambient temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
tCSDOD	Propagation delay time, CS falling edge to DOUT driven DOUT load = 20 pF 100 kΩ to GND			
tDOPD	Propagation delay time, SCLK rising edge to valid new DOUT DOUT load = 20 pF 100 kΩ to GND	0	50	ns
tCSDOZ	Propagation delay time, CS rising edge to DOUT high impedance DOUT load = 20 pF 100 kΩ to GND		100	ns

时序要求
通常是建立时间和保持
时间

开关特性通常是传播
延迟

SPI Timing Diagram

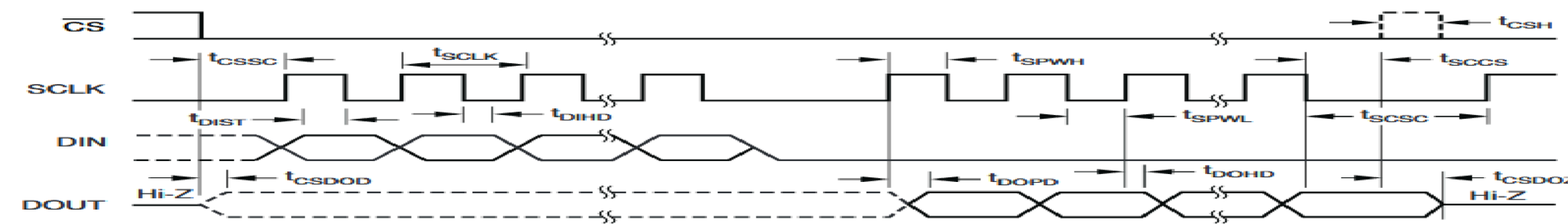


Figure 1. Serial Interface Timing

Timing diagram for the ADS1118

Device uses SPI Mode 1: SCLK idles low, data clocked in at falling edge of SCLK

Boxes for DIN and DOUT are high or low data

Arrows enclose timing specifications

Continuing with the example, here is the timing diagram. We can go through the specifications and explain how to read them. The timing diagram shows specific timing requirements between the different digital lines. For all digital communications, this timing must be followed, or the device may not recognize commands, fail to understand the configuration settings, or properly output data.

We'll cover each of these specifications, and explain what they mean.

SPI 时序图

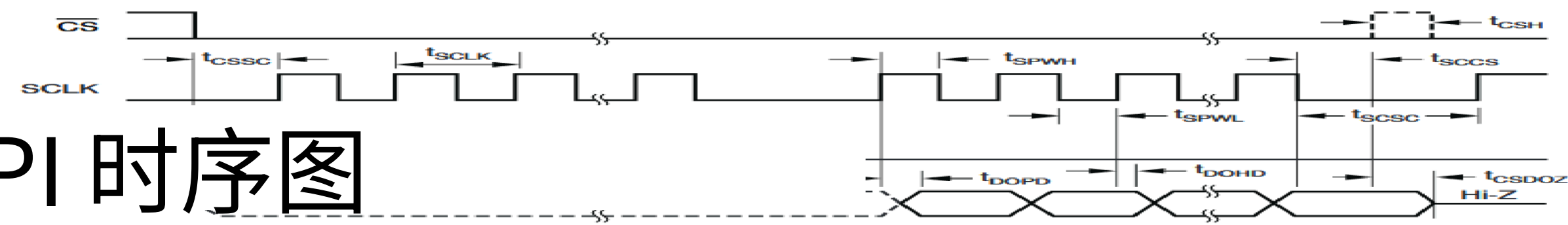


Figure 1. Serial Interface Timing

ADS1118 的时序图



设备使用 SPI 模式 1: SCLK 空闲低电平, 数据在 SCLK 下降沿时钟输入 DIN 和 DOUT 的方框表示数据为高或低电平 箭头包围时序规范

SPI Timing Diagram

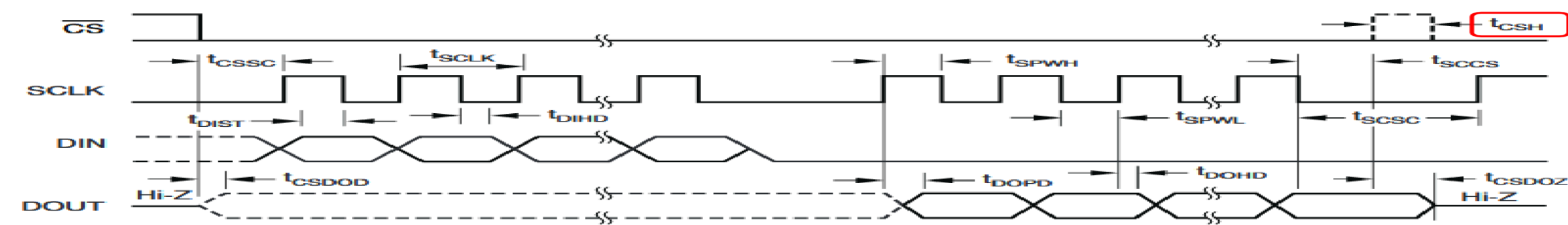


Figure 1. Serial Interface Timing

t_{CSH}

Minimum pulse duration, CS high

This time defines the time required for the CS to stay high to ensure that the device has reset the SPI communications.

t_{CSH} is the hold time of chip select. This is the minimum amount of time that chip select can be held high that ensures that the device recognizes that the chip select has been set high and low again. Here, it does not appear to be a hold time because it does not come before a clock signal in the diagram. However, this timing is internal and defines a hold time based on latching the CS signal to an internal clock.

SPI 时序图

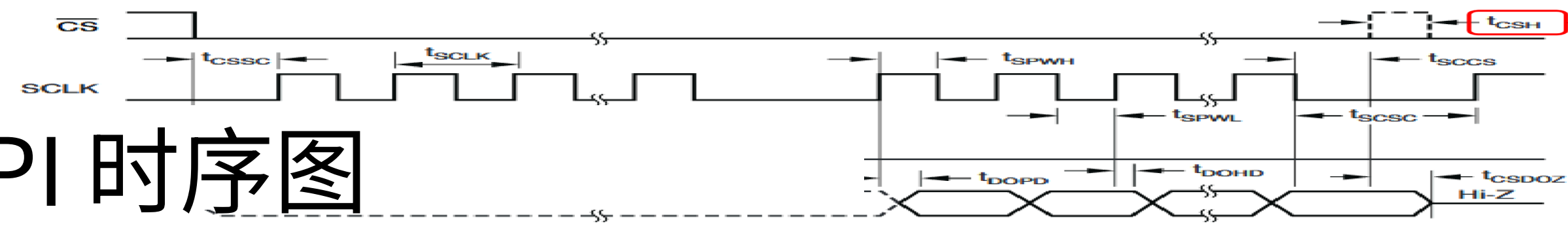


Figure 1. Serial Interface Timing

t

TEXAS INSTRUMENTS

最小脉冲持续时间，CS 高 这个时间定义了 CS 需要保持高电平的时间，以确保设备重置了 SPI 通信。

SPI Timing Diagram

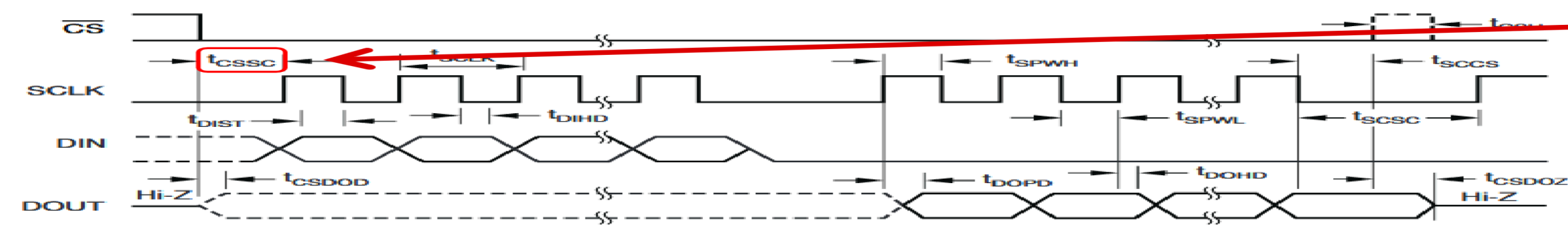


Figure 1. Serial Interface Timing

t_{CSSC}

CS low to first SCLK high

This time defines the time required for the CS to stay high to ensure that the device recognizes it is the peripheral.

A violation may cause the device to miss the first SCLK pulse

t_{CSSC} is the minimum time required between chip select transitioning low and the first SCLK. As chip select is taken low, it still takes a small amount of time for the device to determine that it is the active peripheral. This also allows for time to setup data that the device needs to send out on DOUT at the first SCLK rising edge pulse.

SPI 时序图

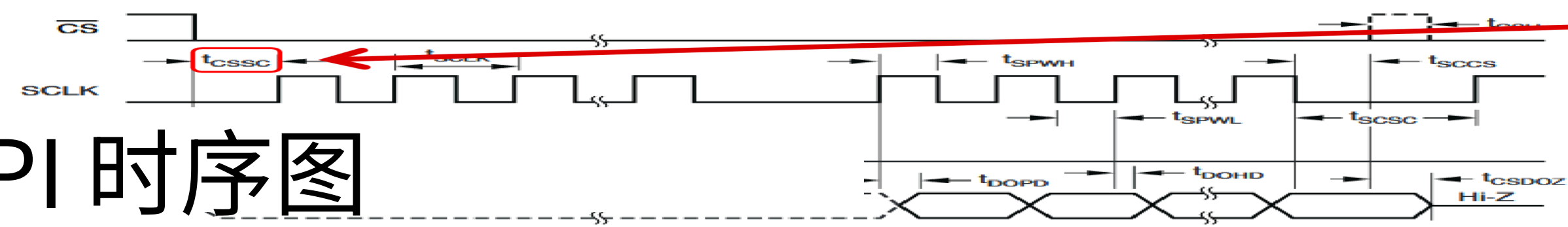


Figure 1. Serial Interface Timing

t

TEXAS INSTRUMENTS

CS 低到第一个 SCLK 高这段时间定义了 CS 保持高电平所需的时间，以确保设备识别其为外设。违反此规定可能导致设备错过第一个 SCLK 脉冲

SPI Timing Diagram

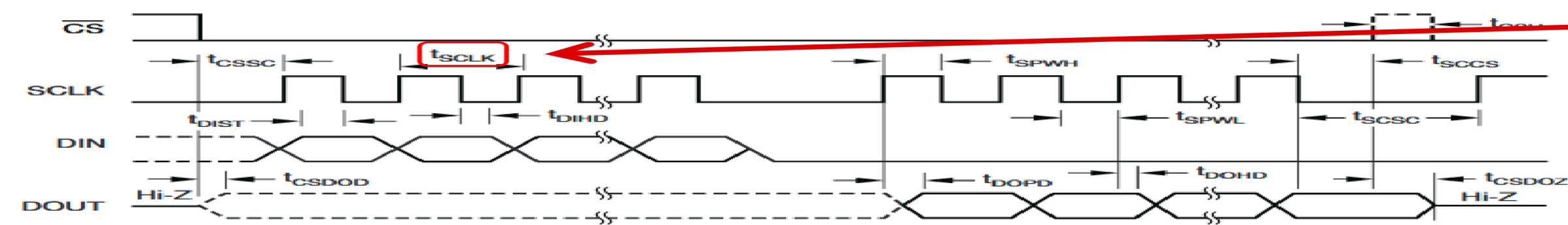


Figure 1. Serial Interface Timing

t_{SCLK}

The minimum time for an SCLK period

SCLKs can be sent to a device only so fast before the device fails to recognize it. This defines the minimum time for SCLK.

$1/t_{SCLK}$ is the SCLK frequency

t_{SCLK} is the SCLK period. SCLK must have a minimum period to ensure proper digital timing. Transistors and logic gates can't be clocked infinitely fast, so there is a limit to how fast data can be clocked out.

SPI 时序图

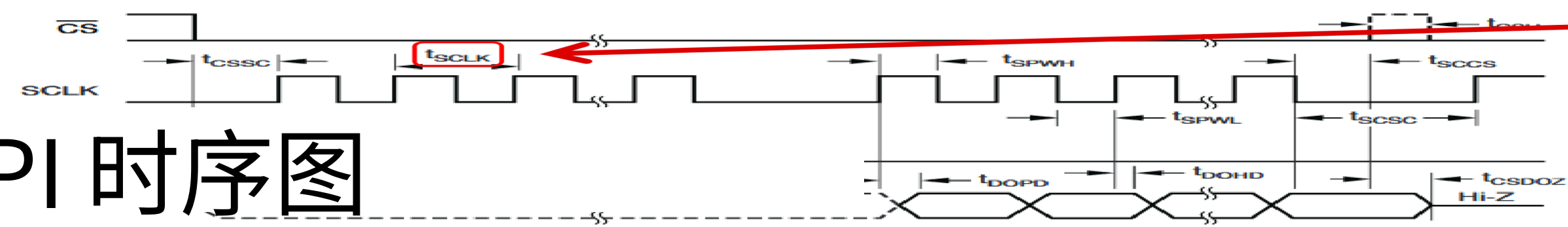


Figure 1. Serial Interface Timing

t

SCLK 周期的最小时间 SCLK 只能以多快的速度发送到设备，否则设备将无法识别。这定义了 SCLK 的最小时间。 $1/t_i$ 是 SCLK 频率

SPI Timing Diagram

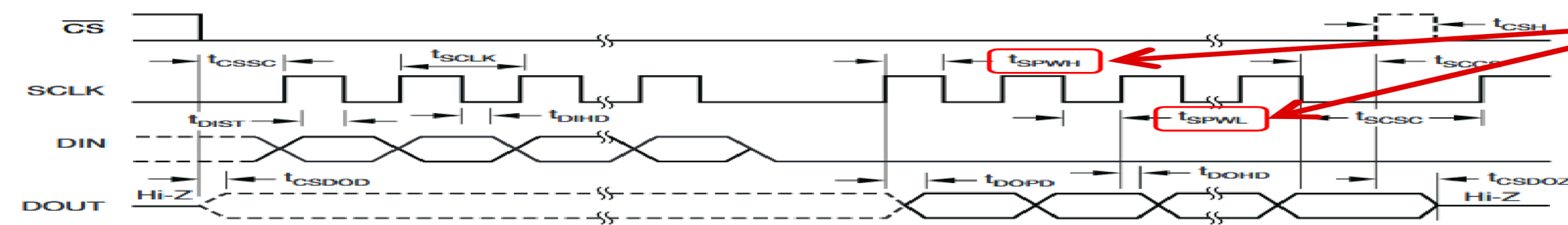


Figure 1. Serial Interface Timing

t_{SPWH} , t_{SPWL}

The minimum time for an SCLK high and the minimum time for an SCLK low

These two times with t_{SCLK} define how much skew in the SCLK duty cycle is allowed

For this device, there is a maximum t_{SPWL} for SPI timeout

t_{SPWH} and t_{SPWL} are the minimum time periods for the SCLK pulse high and low. This is similar to the total minimum SCLK period, but it really describes the acceptable duty cycle and skew of the SCLK signal.

For this timing specification, there is an additional limit. The timing requirement table lists a maximum t_{SPWL} time of 28ms. This maximum time comes from a timeout built into the SPI communications of this device.

SPI 时序图

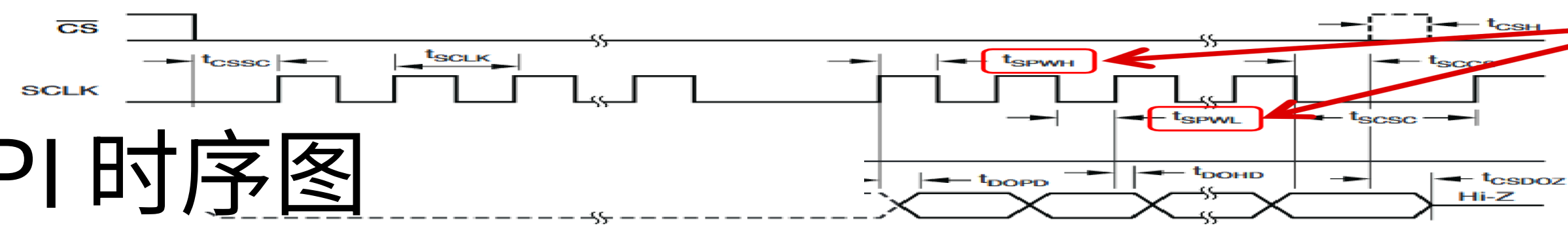


Figure 1. Serial Interface Timing

t, t

SCLK 高电平的最小时间和 SCLK 低电平的最小时间，这两个时间与 t 共同定义了 SCLK 占空比允许的偏移量。对于此设备，存在一个 SPI 超时的最大 t 值

SPI Timing Diagram

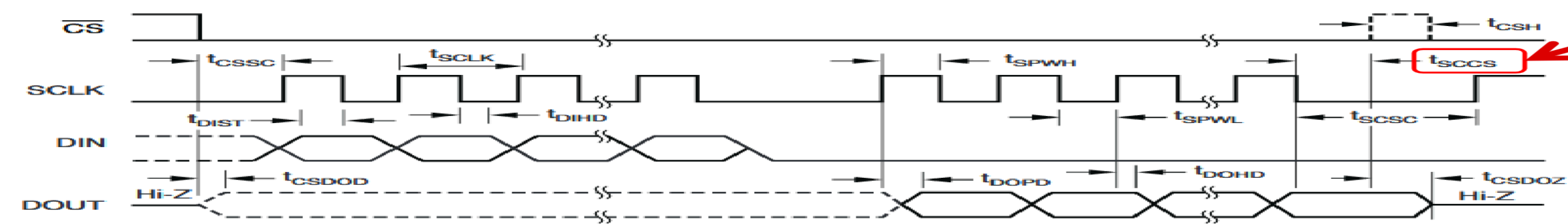


Figure 1. Serial Interface Timing

t_{SCCS}

Time from the falling edge of SCLK to the rising edge of CS

Because CS disables the SPI, ensure that the device receives the last bit of data before shutting down SPI communication

A violation of this could cause the device to miss the last data transmission

t_{SCCS} is the minimum time from the last SCLK falling edge to the rising edge of chip select. This is a specification required for clocking in data to the device. Because chip select disables the SPI communication, any data must be clocked into the device with the falling edge of SCLK before chip select rises. It is a hold time for the data with SCLK and a setup time for the chip select to the device's internal clock.

SPI 时序图

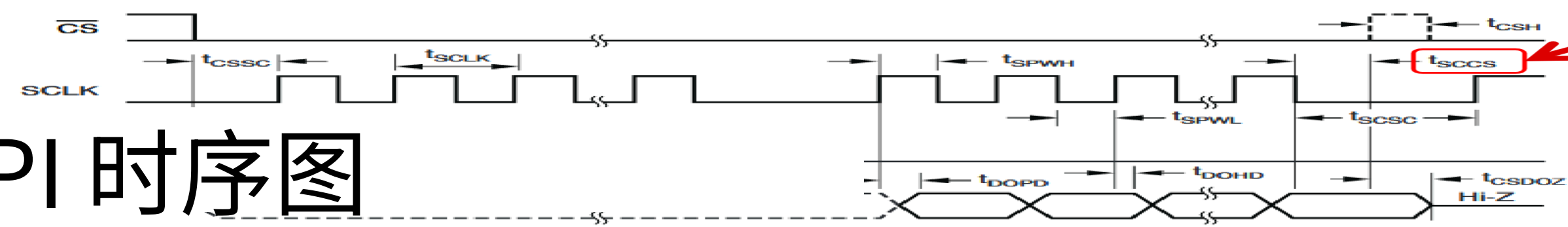


Figure 1. Serial Interface Timing



t

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从 SCLK 的下降沿到 CS 的上升沿的时间 因为 CS 禁用了 SPI，所以确保

设备在关闭 SPI 通信之前接收最后一位数据。违反这一规定可能会导致设备错过最后的数据传输

SPI Timing Diagram

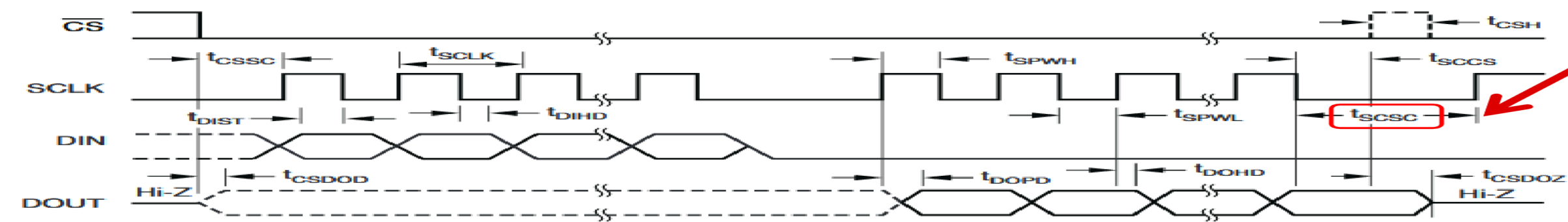


Figure 1. Serial Interface Timing

t_{SCSC}

Time from the falling edge of SCLK to the rising edge of SCLK in the next CS

This time is required to execute the command from one CS period, to start a new command in another CS period



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13

t_{SCSC} is the time required between the last falling edge of SCLK from one command to the next rising edge of SCLK for the next command. For the device, there is some time required to parse and execute a command in one chip select frame before being able to take another command from another chip select frame.

SPI 时序图

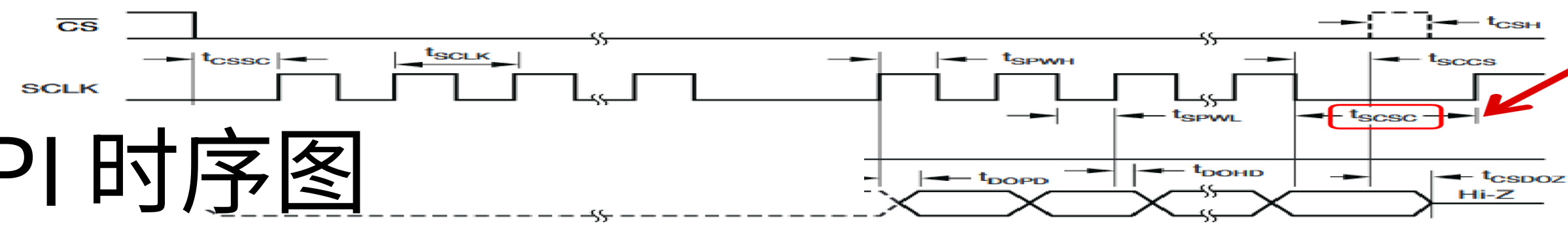


Figure 1. Serial Interface Timing

t

TI TEXAS INSTRUMENTS

从 SCLK 下降沿到下一个 $\overline{CS}$ 的 SCLK 上升沿的时间。这段时间用于在一个 CS 周期内执行命令，并在另一个 CS 周期内开始新命令

SPI Timing Diagram

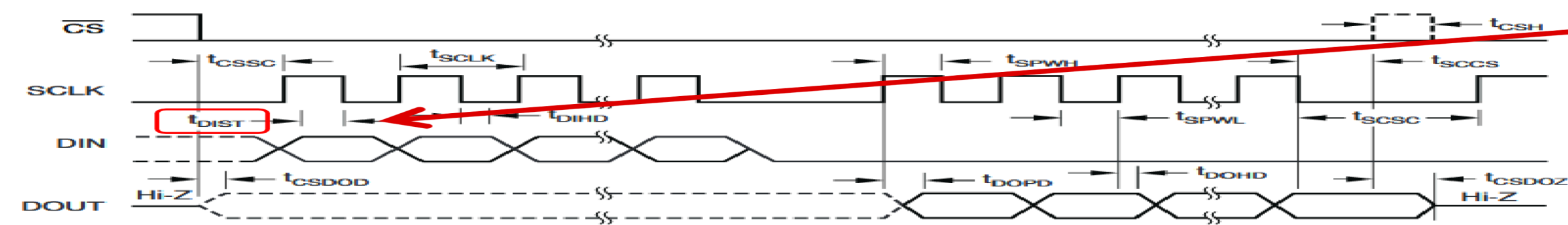


Figure 1. Serial Interface Timing

t_{DIST}

Setup time from the rising edge of DIN to the falling edge of SCLK

For data to be read into the device, the DIN must first be established for a time period before the SCLK falling edge.

t_{DIST} is the setup time for the DIN data. In this diagram, the communication uses SPI mode 1, where the SCLK idles low and data are clocked in on the falling edge of SCLK. Here, the DIN is typically set up on the rising edge of SCLK, but this defines a minimum time that DIN must be valid before the falling edge of SCLK.

Again, this device is SPI mode 1, where the data is clocked in at the falling edge of SCLK. The setup time is the time required for DIN to be stable, before the active falling SCLK edge.

SPI 时序图

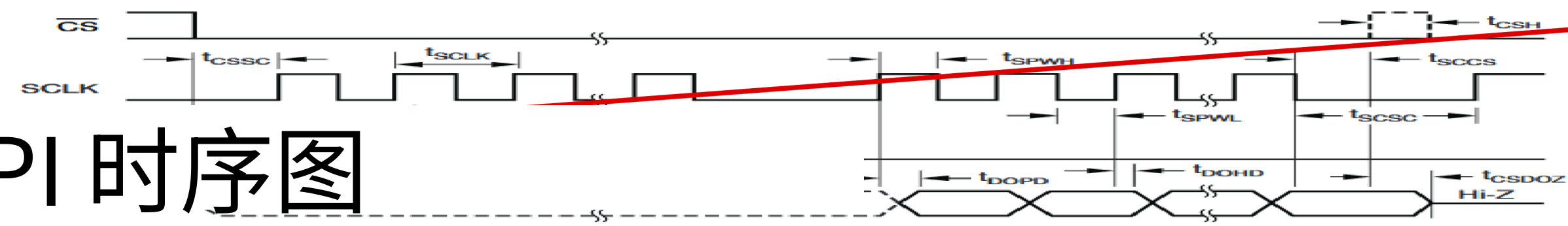


Figure 1. Serial Interface Timing

t

从 DIN 的上升沿到 SCLK 的下降沿的建立时间 为了让数据被读入设备，DIN 必须在 SCLK 下降沿之前建立一段时间。

SPI Timing Diagram

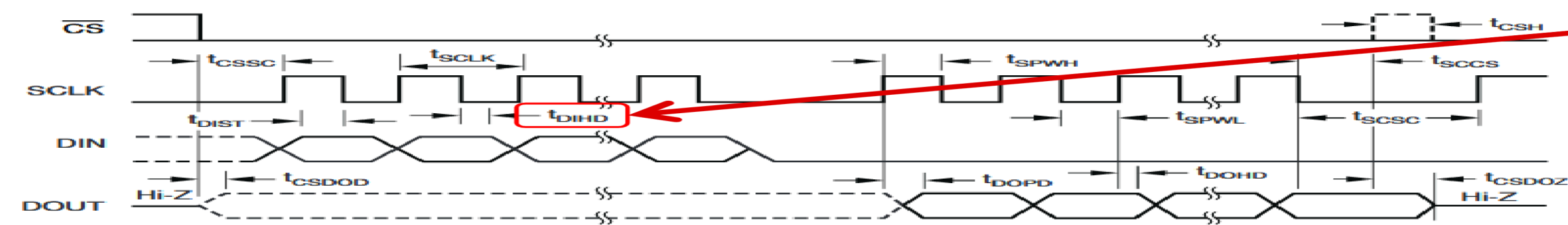


Figure 1. Serial Interface Timing

t_{DIHD}

Hold time from the falling edge of SCLK to the falling edge of DIN.

Once the data is set onto the DIN line, the SCLK falling edge latches the data into the device. However, there is a required time for the data to be held after the SCLK falling edge

t_{DIHD} is the hold time for the DIN data. When the data is clocked in on the falling edge of SCLK, DIN must be stable from the setup time before and the hold time after the SCLK falling edge.

SPI 时序图

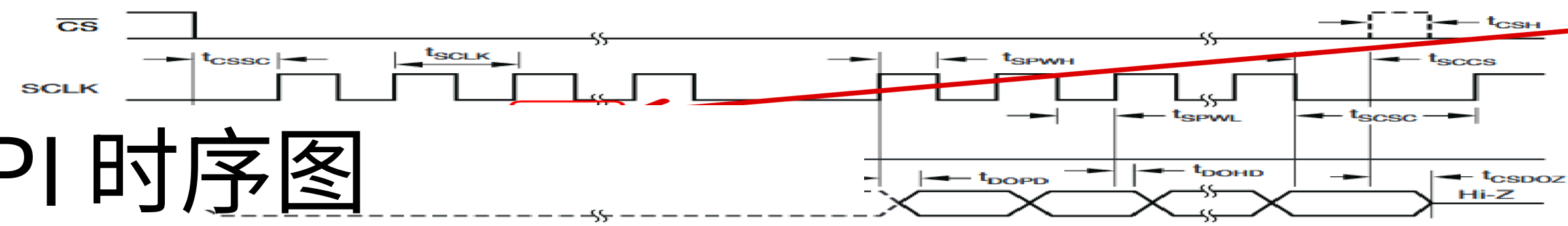


Figure 1. Serial Interface Timing

t

从 SCLK 的下降沿到 DIN 的下降沿的保持时间。一旦数据被设置到 DIN 线上，SCLK 的下降沿将数据锁存到设备中。然而，在 SCLK 下降沿之后，数据需要保持一段所需的时间

SPI Timing Diagram

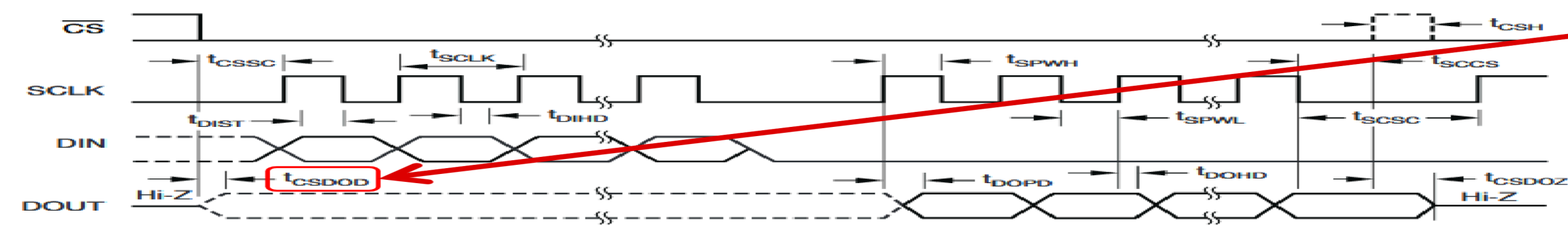


Figure 1. Serial Interface Timing

t_{CSDOD}

Propagation delay time from CS falling to DOUT actively driven

When CS is high, the DOUT is high impedance or Hi-Z, allowing for multiple devices on the bus to drive DOUT a device at a time.

When CS goes low, DOUT is actively driven



TEXAS INSTRUMENTS

16

t_{CSDOD} is the time from the falling edge of chip select to the enabling of DOUT. When chip select is high, the DOUT of the peripheral device is high impedance, or Hi-Z. This prevents an inactive peripheral device from trying to drive the DOUT line. When chip select is driven low, DOUT is driven by the active peripheral. t_{CSDOD} shows the propagation delay from the chip select going low to when the DOUT is active.

SPI 时序图

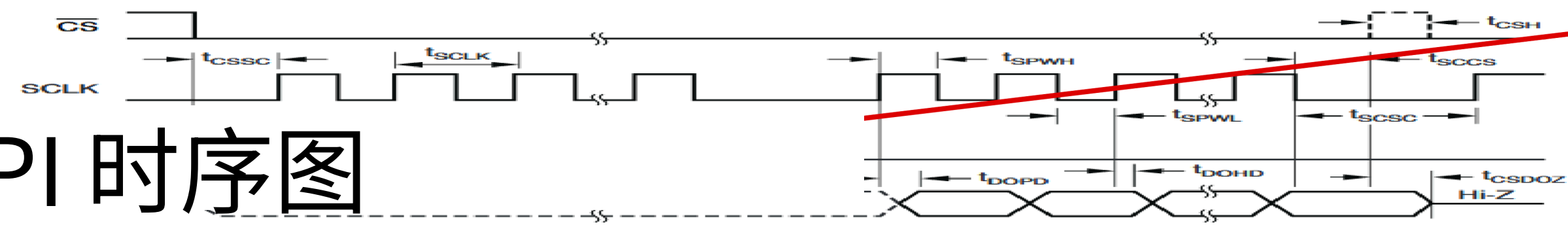


Figure 1. Serial Interface Timing

t

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CS 下降沿到 DOUT 主动驱动的传播延迟时间。当 CS 为高电平时，DOUT 为高阻抗或 Hi-Z 状态，允许总线上多个设备逐个驱动 DOUT。

当 CS 变为低电平时，DOUT 被主动驱动

SPI Timing Diagram

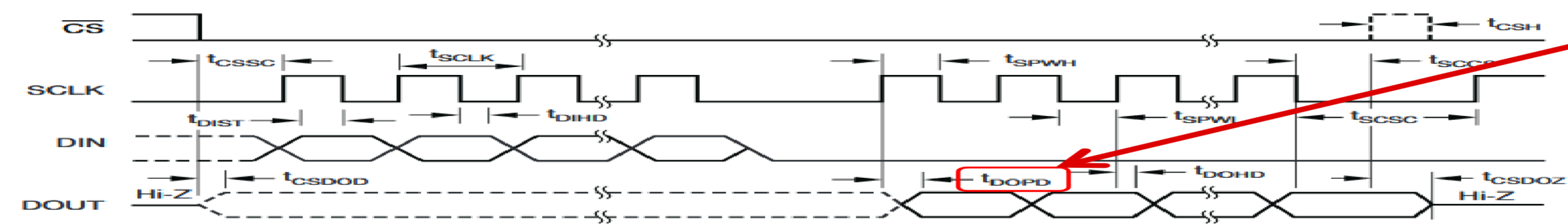


Figure 1. Serial Interface Timing

t_{DOPD}

Propagation delay time from rising edge of SCLK to data appearing on DOUT

SCLK is used to clock out data from the device. When SCLK is driven high, this signals to the device that data should be put on DOUT that can be clocked out on the falling edge of DOUT

t_{DOPD} is the maximum propagation delay time from the rising edge of SCLK to the data appearing on DOUT. Again, data is clocked out by the controller on the falling edge of SCLK, so the rising edge of SCLK is used by the device to send data to DOUT.

SPI 时序图

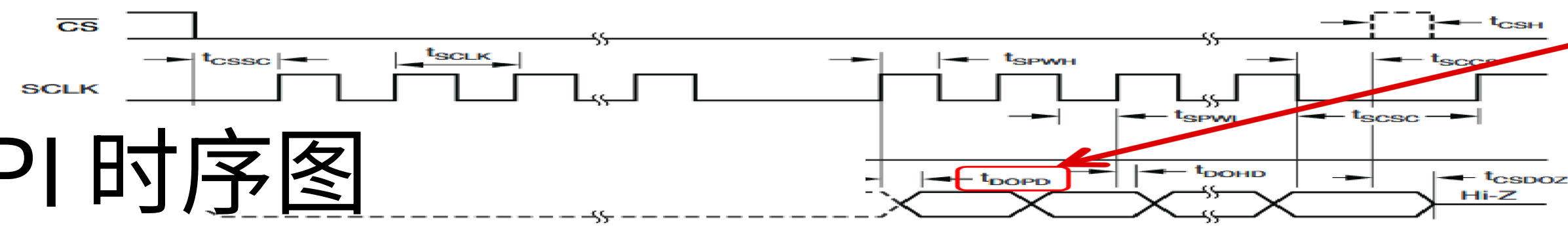


Figure 1. Serial Interface Timing



从 SCLK 的上升沿到 DOUT 上数据出现的传播延迟时间用于从设备中时钟输出数据。当 SCLK 被驱动为高电平时，这会向设备发出信号，表示数据应该被放到 DOUT 上，该数据可以在 DOUT 的下降沿被时钟输出。

SPI Timing Diagram

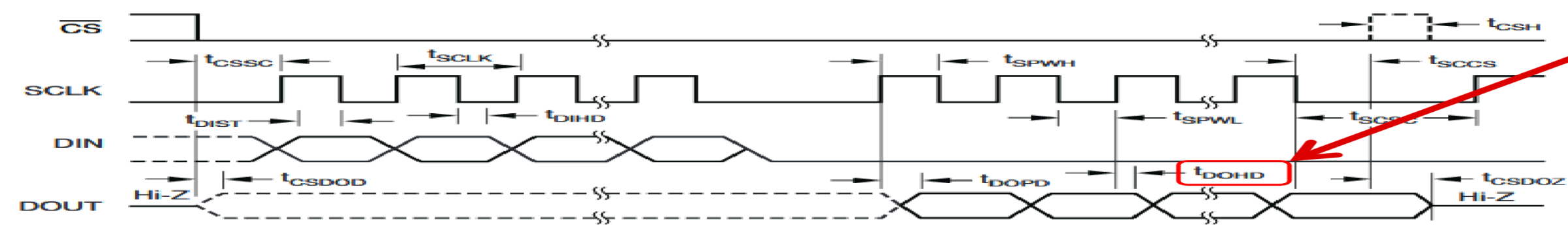


Figure 1. Serial Interface Timing



**Propagation delay time
from rising edge of SCLK
to data changing on
DOUT**

This defines the time for which the last data is still valid once the rising edge of SCLK occurs

tDOHD is the propagation delay time from the SCLK rising edge to when DOUT becomes invalid. Again, DOUT is set up on the rising edge of SCLK so that it can be read out on the falling edge of SCLK. However, if you choose to read the data, you have until tDOHD after the next rising edge of SCLK to read the data.

This specification isn't important if the data is read on the falling edge of SCLK.

SPI 时序图

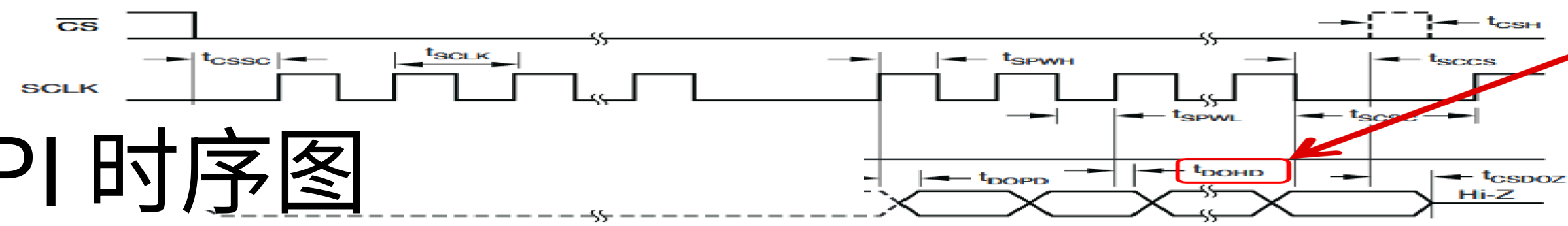


Figure 1. Serial Interface Timing

t

从 SCLK 的上升沿到 DOUT 上数据变化的传播延迟时间。这定义了 SCLK 上升沿发生后，最后的数据仍然有效的持续时间。

SPI Timing Diagram

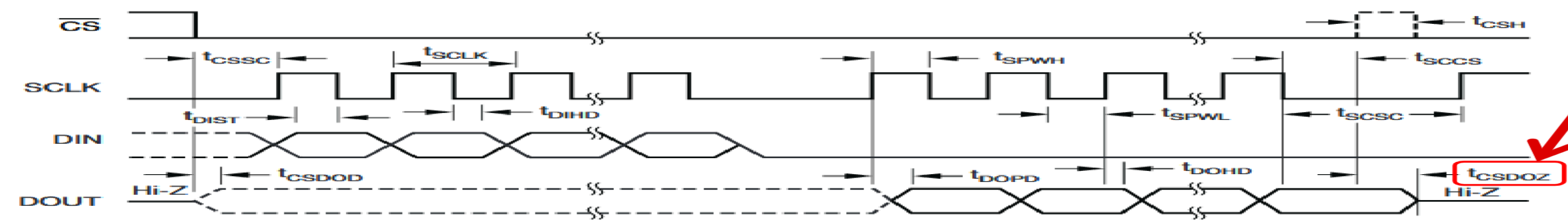


Figure 1. Serial Interface Timing

t_{CSDOZ}
Propagation delay time from rising edge of CS to DOUT becoming Hi-Z

t_{CSDOZ} is the time from the rising edge of chip select to when DOUT returns to high impedance. Similar to t_{CSDOD} , this is important when there are peripheral multiple devices on the SPI bus.

SPI 时序图

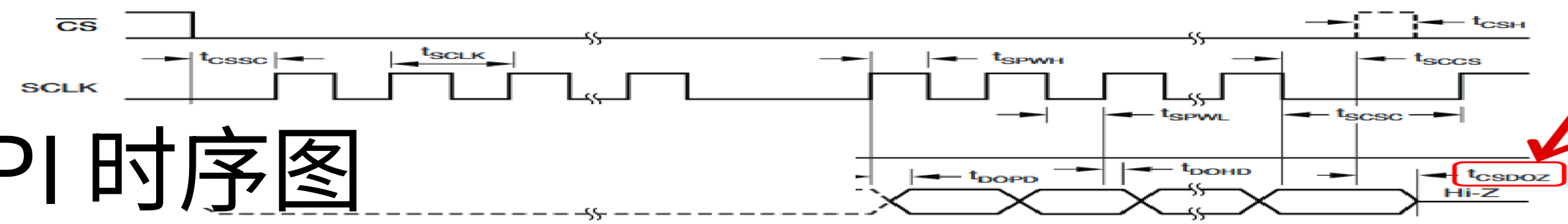


Figure 1. Serial Interface Timing

t

CS 上升沿到 DOUT 变为高阻态的传播延迟时间

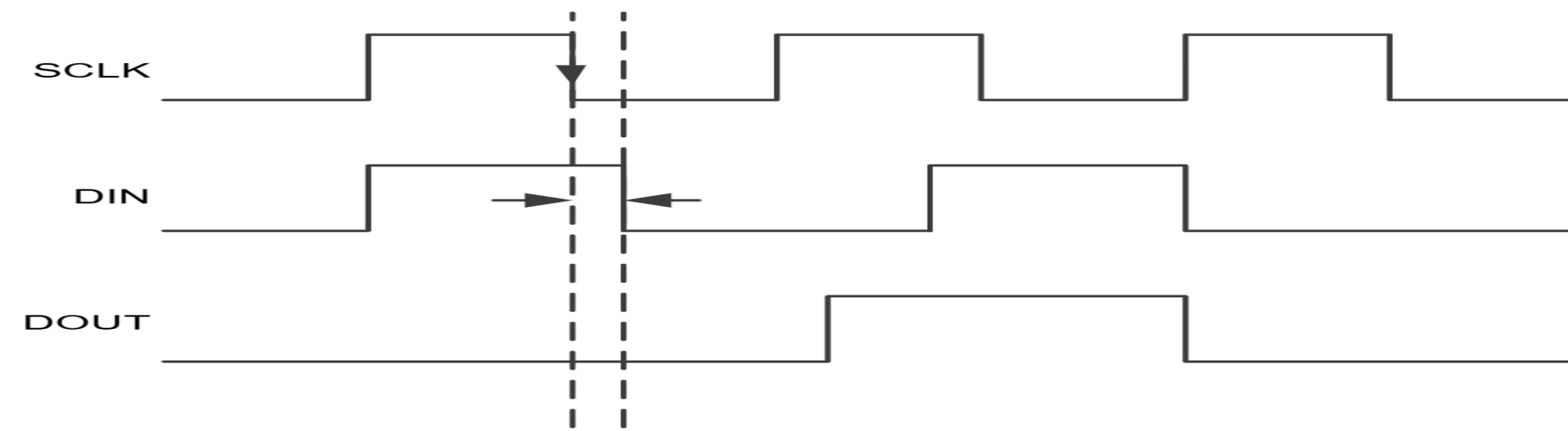
Thanks for your time! Please try the quiz.

That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video’s content.

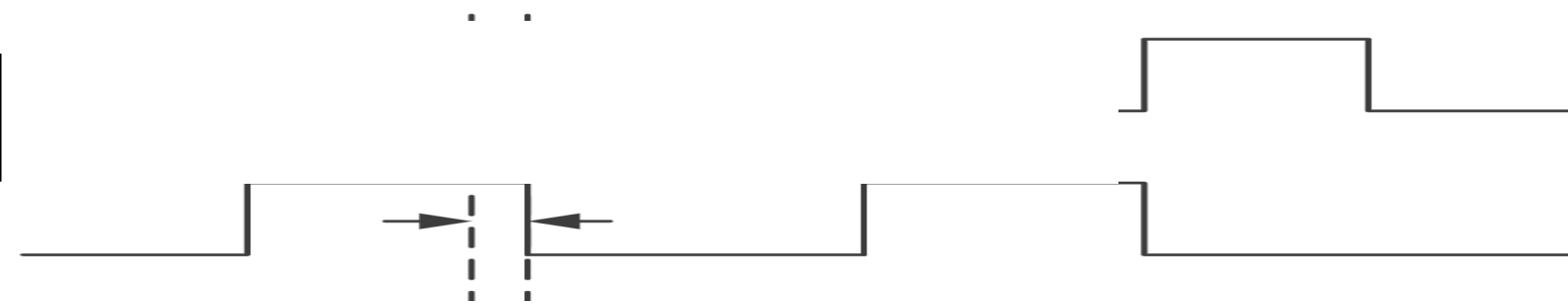
感谢您的时间！ 请尝试测验。

Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
- a. Setup time
 - b. Hold time
 - c. Propagation delay
 - d. None of the above



测验：SPI 基础：时序图



1. 如下图表为 $CPOL = 0$, $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿后保持稳定。这个时序是哪种时序要求的一个例子？



- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

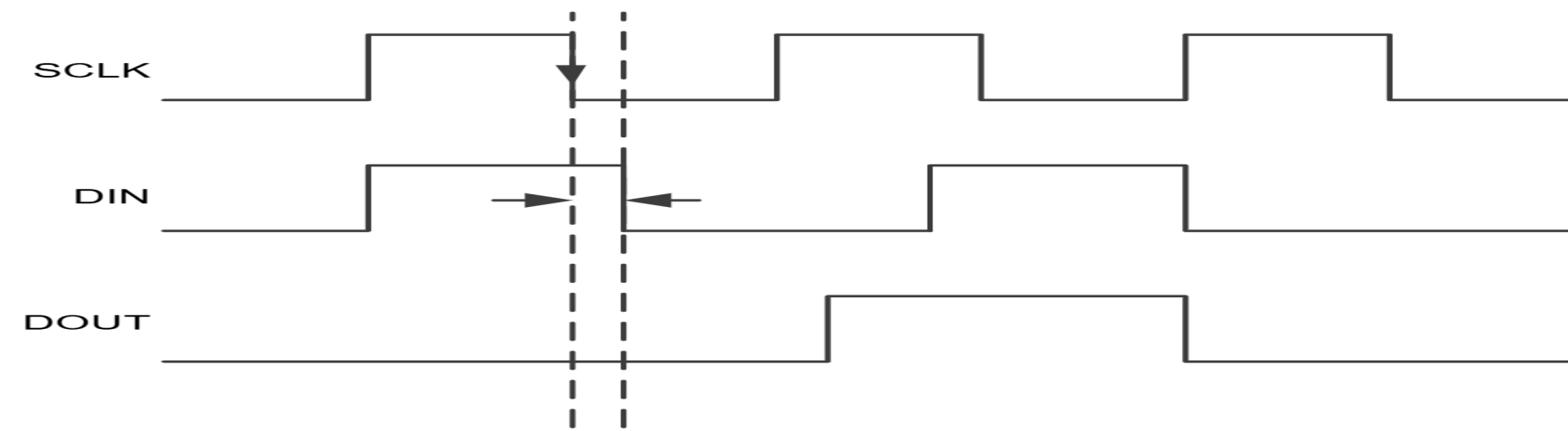
SCLK

DIN

DOUT

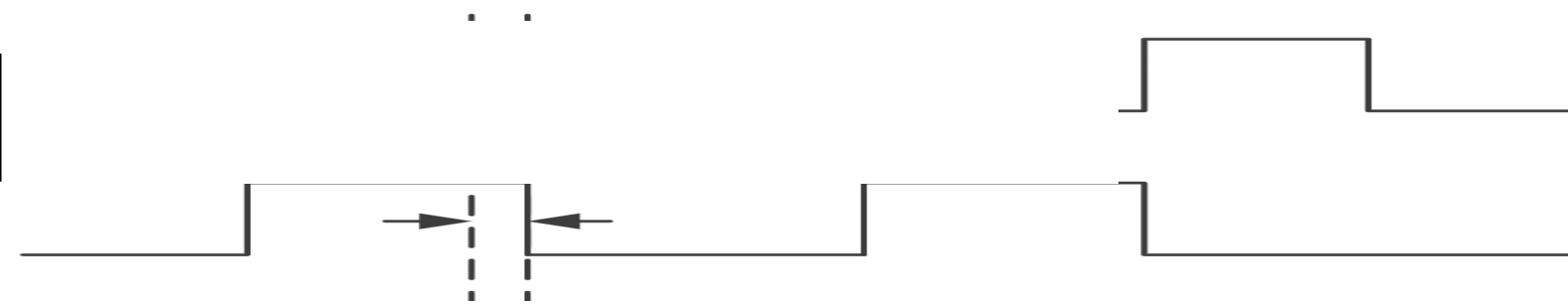
Quiz: Basics of SPI: Timing Diagram

1. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time after the SCLK falling edge. This timing is an example of which timing requirement?
- a. Setup time
 - b. Hold time**
 - c. Propagation delay
 - d. None of the above



B. Hold time. The SCLK is clocks in data on a falling edge. Here we see that we want to clock in DIN to the peripheral on the SCLK falling edge. This timing diagram shows the amount of time that is required to hold DIN after the falling edge of SCLK.

测验：SPI 基础：时序图



1. 如下图表为 $CPOL = 0$, $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿后保持稳定。这个时序是哪种时序要求的一个例子？



- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

SCLK

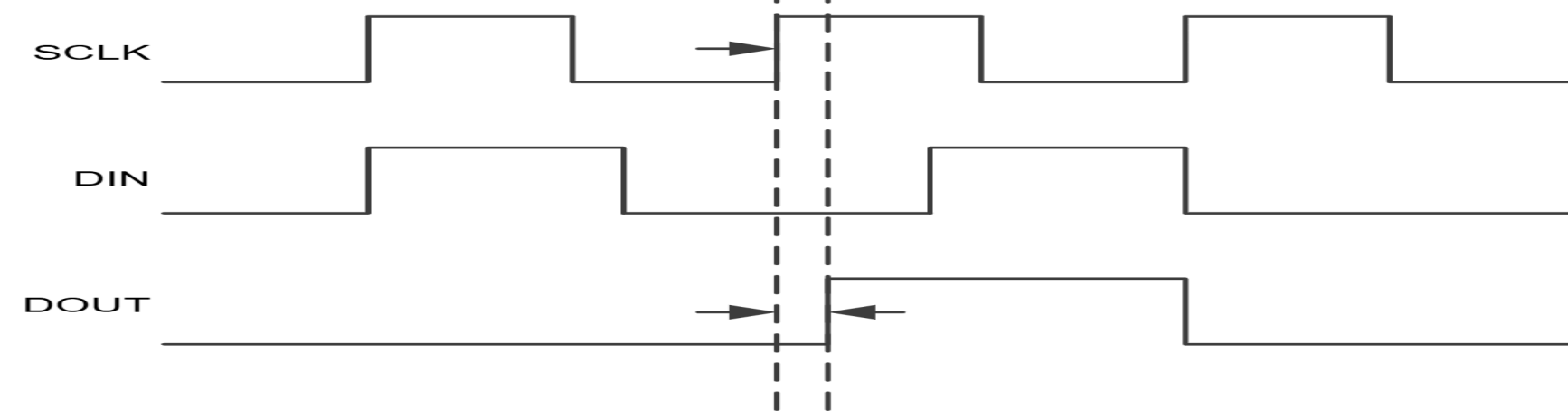
DIN

DOUT

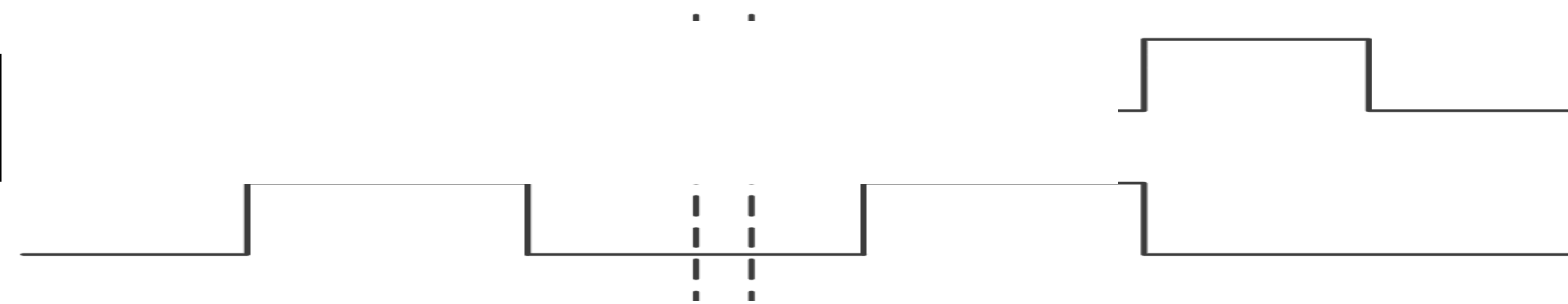
Quiz: Basics of SPI: Timing Diagram

2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



测验：SPI 基础：时序图



2. 下列图表中 $CPOL = 0$ ， $CPHA = 1$ 。DIN 和 DOUT 在 SCLK 的下降沿读取。然而 DOUT 在 SCLK 的上升沿建立，并且数据到达 DOUT 可能需要时间。这种时序是哪种时序要求？

IENTS

- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

SCLK

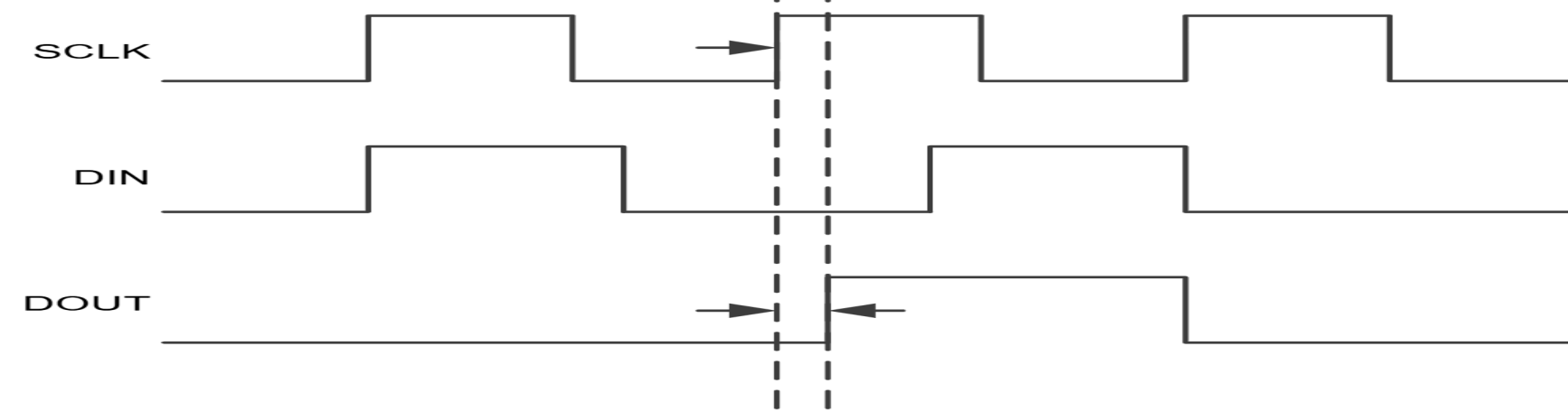
DIN

DOUT

Quiz: Basics of SPI: Timing Diagram

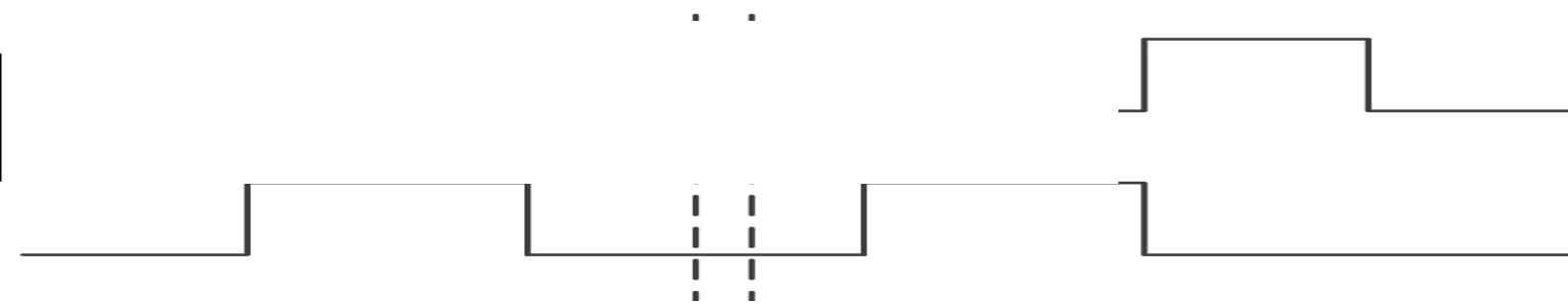
2. The following diagram is CPOL = 0, CPHA = 1. DIN and DOUT are read on the falling edge of SCLK. However, DOUT is set up on the rising edge of SCLK, and there may be time required for the data to arrive on DOUT. This timing is an example of which timing requirement?

- a. Setup time
- b. Hold time
- c. Propagation delay
- d. None of the above



C. Propagation delay. In this diagram data is set up on the rising edge of the SCLK and clocked in the peripheral or controller on the falling edge. Here, the SCLK rising edge tells the peripheral to get the data out to DOUT so that it can be latched into the controller on the falling edge. This is a propagation delay showing the amount of time required from the rising edge of SCLK to get data out on DOUT.

测验：SPI 基础：时序图



2. 下列图表中 $CPOL = 0$, $CPHA = 1$ 。DIN 和 DOUT 在 SCLK 的下降沿读取。然而 DOUT 在 SCLK 的上升沿建立，并且数据到达 DOUT 可能需要时间。这种时序是哪种时序要求？

IENTS

- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

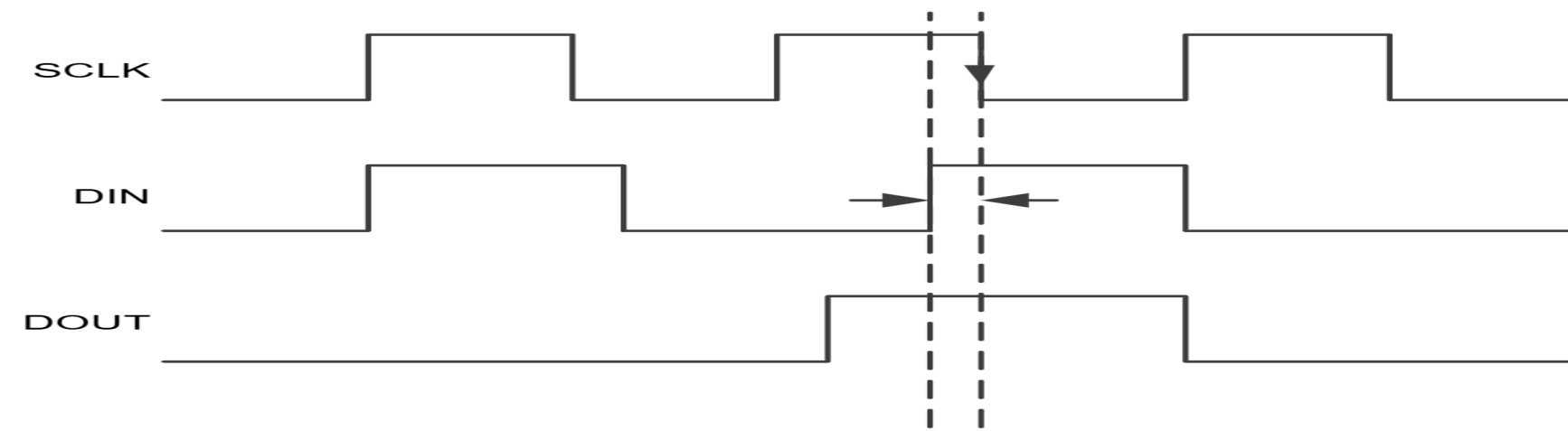
SCLK

DIN

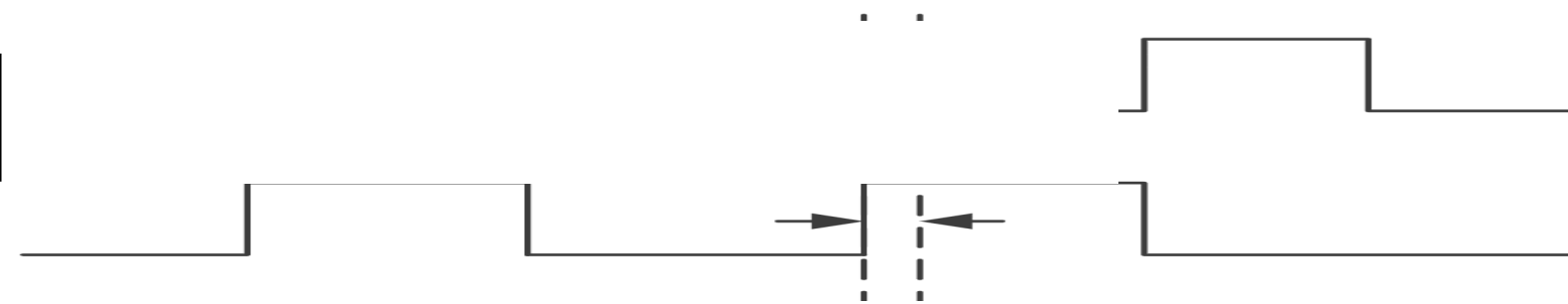
DOUT

Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
- a. Setup time
 - b. Hold time
 - c. Propagation delay
 - d. None of the above



测验：SPI 基础：时序图



3. 如下所示为 $CPOL = 0$, $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿之前保持稳定。这种时序是哪种时序要求的一个例子？



- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

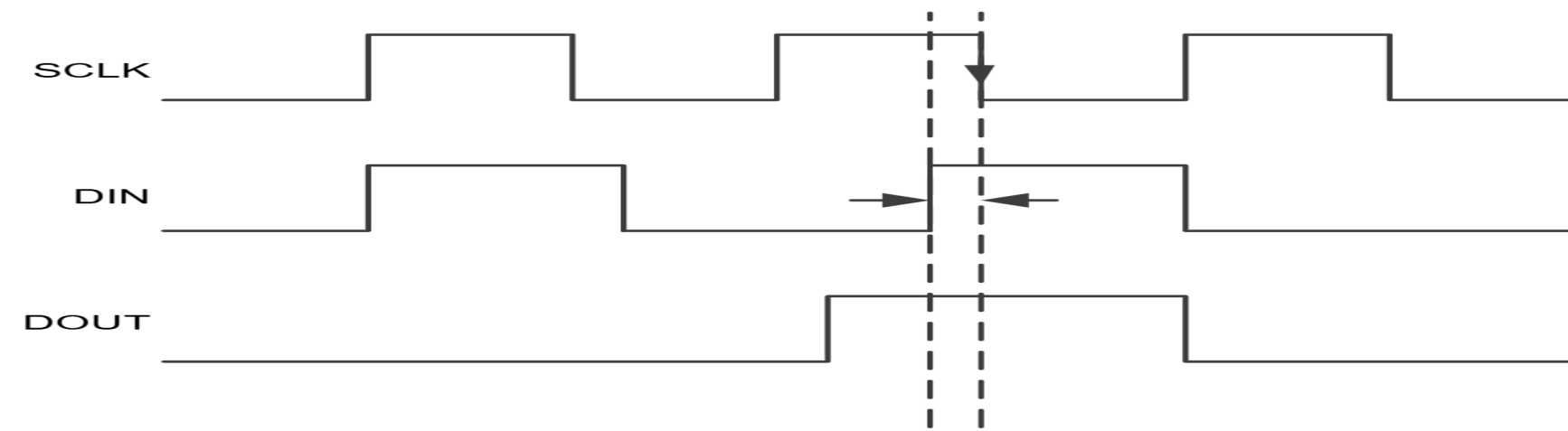
SCLK

DIN

DOUT

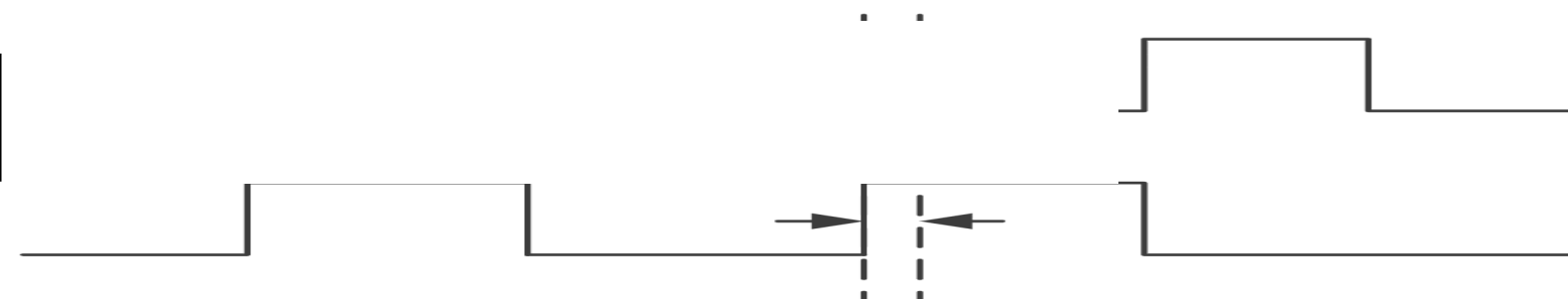
Quiz: Basics of SPI: Timing Diagram

3. The following diagram is CPOL = 0, CPHA = 1. Data is clocked in on the falling edge of SCLK. DIN must be stable for a time before the falling edge of SCLK. This timing is an example of which timing requirement?
- a. Setup time
 - b. Hold time
 - c. Propagation delay
 - d. None of the above



A. Setup time. Data is latched on the falling edge of SCLK. This setup time defines how much time is required to that the DIN is set and stable before the falling edge of SCLK.

测验：SPI 基础：时序图



3. 下图是 $CPOL = 0$, $CPHA = 1$ 。数据在 SCLK 的下降沿时钟输入。DIN 必须在 SCLK 下降沿之前保持稳定。这个时序是哪个时序要求的示例？



- a. 建立时间
- b. 持续时间 c. 传播延迟
- d. 以上都不是

SCLK

DIN

DOUT

Thanks for your t

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