What is Clock and Data Recovery (CDR) ?

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什么是时钟和数据恢复（CDR）？

德州仪器精密实验室 – HSSC

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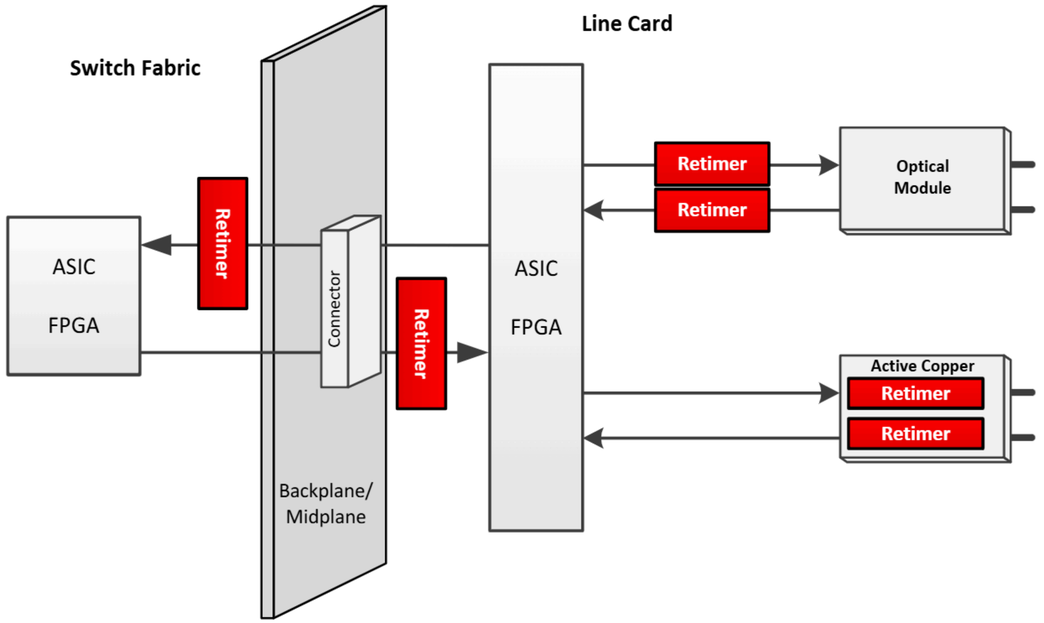
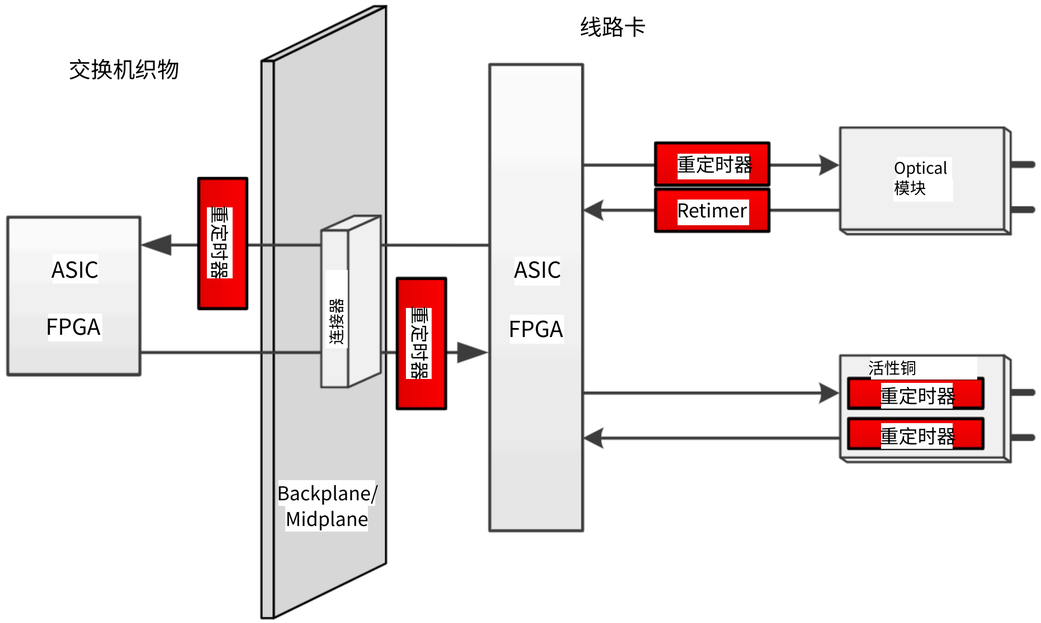
Why are CDR retimers important?



Example retimer system, enterprise networking switch

Clock and data recovery (CDR) in retimers reduce noise and jitter in data signals, extend system link reaches and lower achievable bit error rates and enable system compliance to high-speed standard specifications.

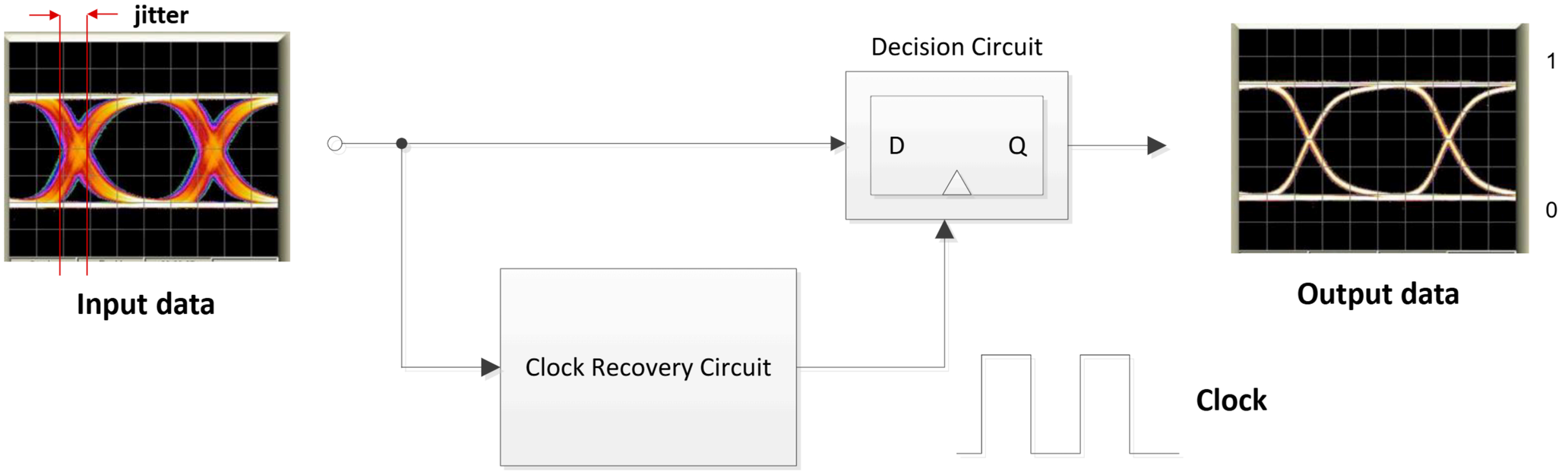
为什么 CDR 再生器很重要?



再定时器系统示例，企业级网络交换机

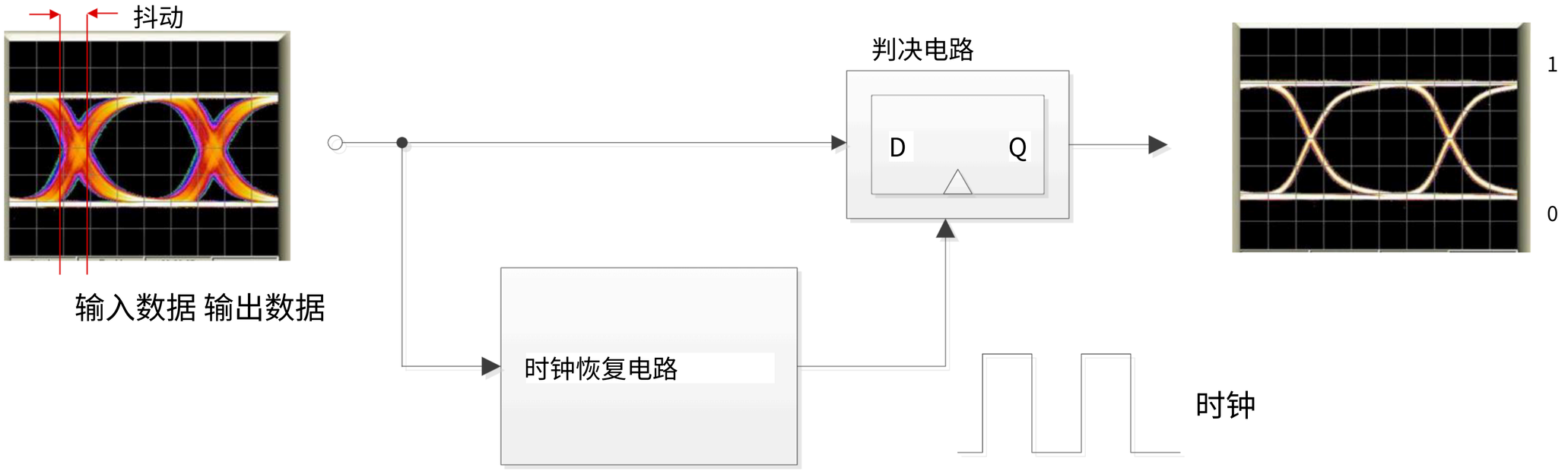
时钟与数据恢复（CDR）在再定时器中减少数据信号中的噪声和抖动，延长系统链路距离，降低可实现的比特错误率，并使系统能够符合高速标准规范。

What function do CDRs perform in retimers?



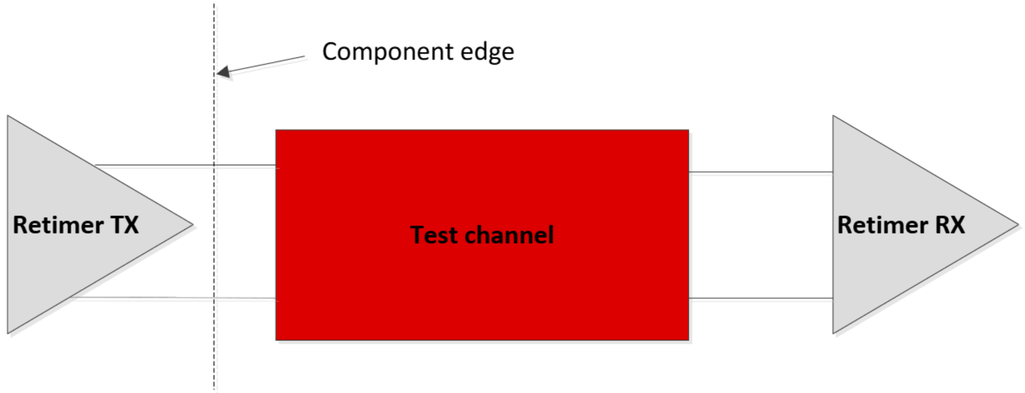
Simplified diagram of a CDR based retimer

CDRs 在再定时器中执行什么功能?

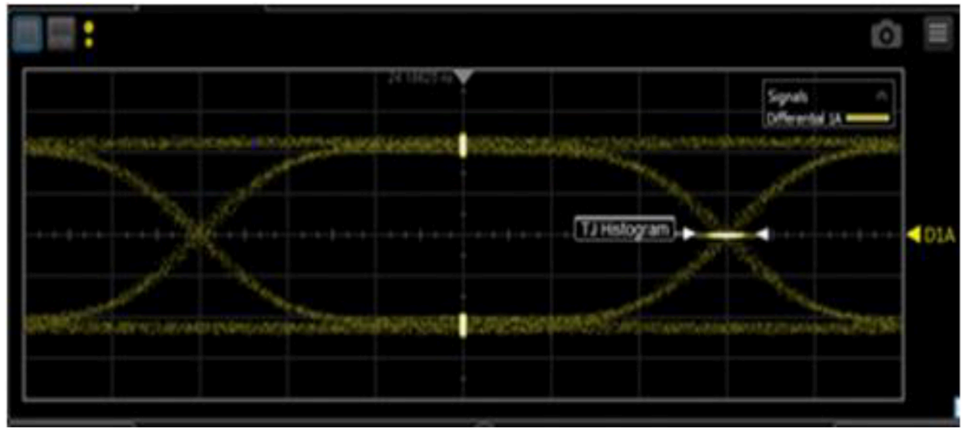


基于 CDR 的再定时器的简化示意图

Retimer with CDR Tx output jitter

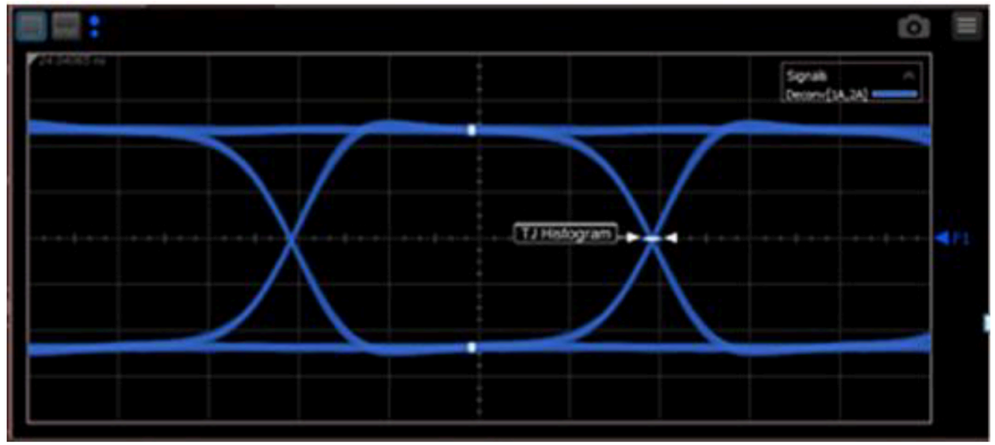


Raw data, CDR bypassed



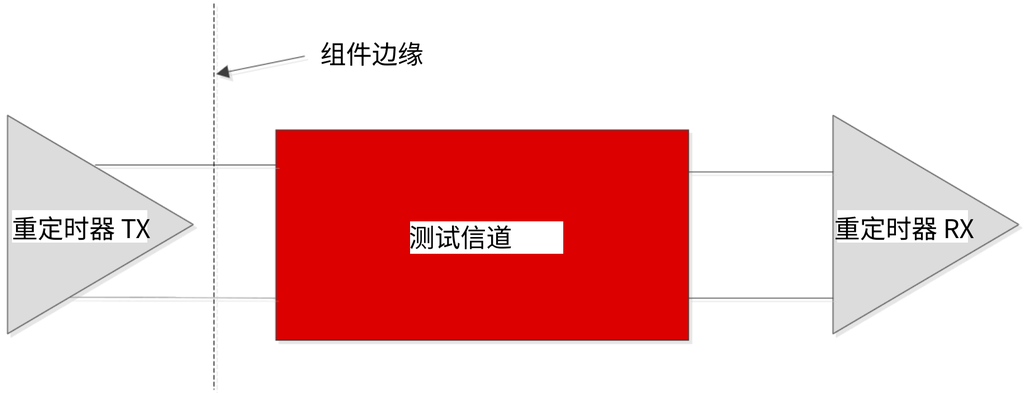
Total jitter = 13.0ps

Retimed data, CDR enabled

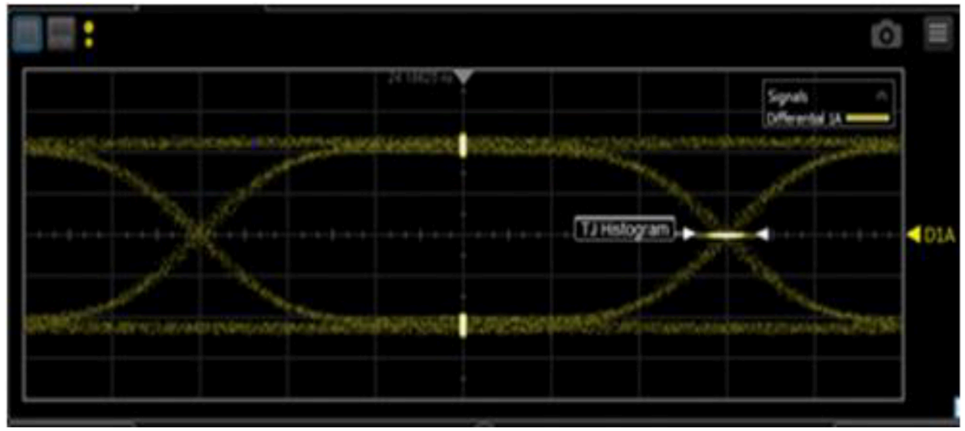


Total jitter = 7.15ps

带 CDR Tx 输出抖动的重定时器

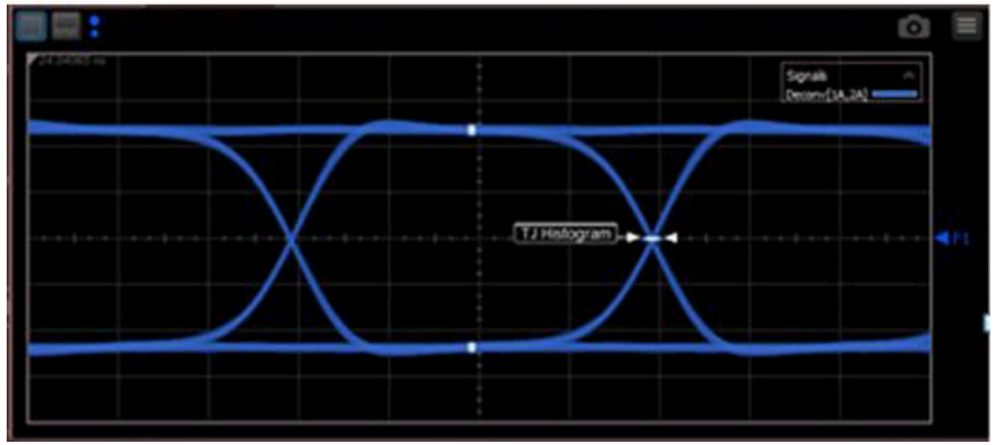


原始数据，CDR 绕过



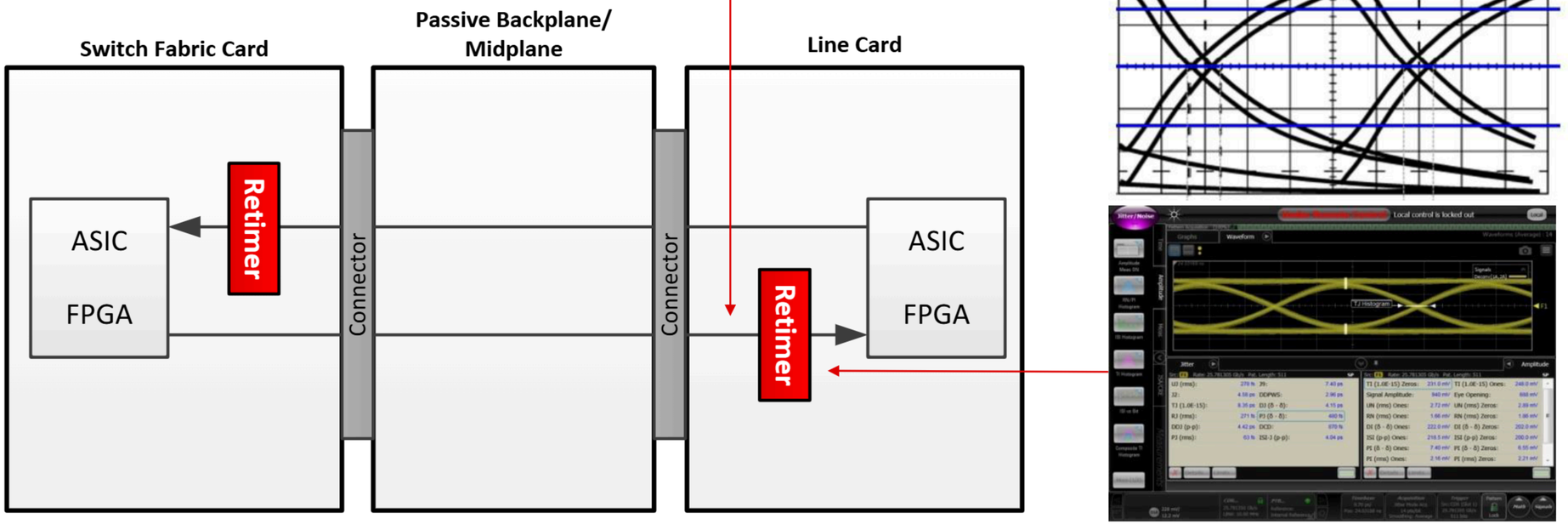
总抖动 = 13.0ps

重定时器数据，CDR 启用



总抖动 = 7.15ps

Choosing a retimer based on CDR performance



Backplane system with retimers

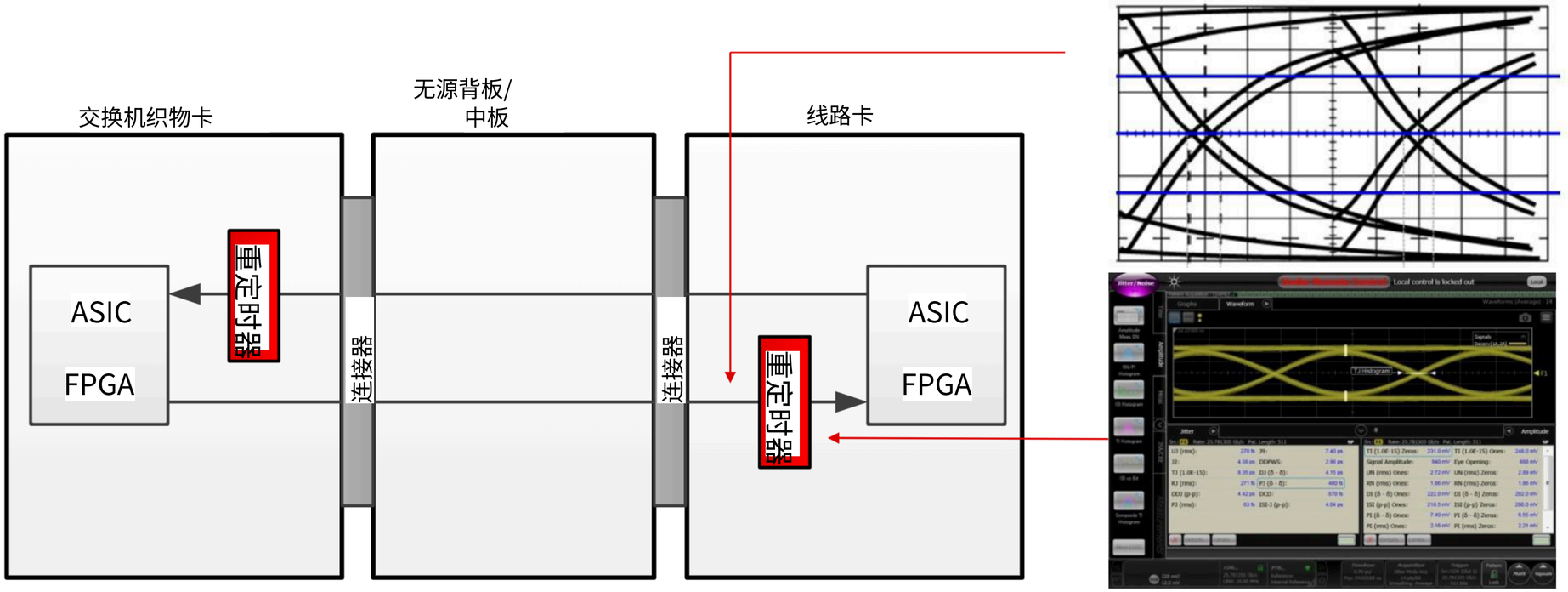
Jitter metrics

- How much jitter stress can CDR handle
- How much jitter propagates to its output

CDR lock behavior

- Data rates supported
- Lock consistency and stability over operating conditions

基于 CDR 性能选择重定时器



带重定时器的背板系统

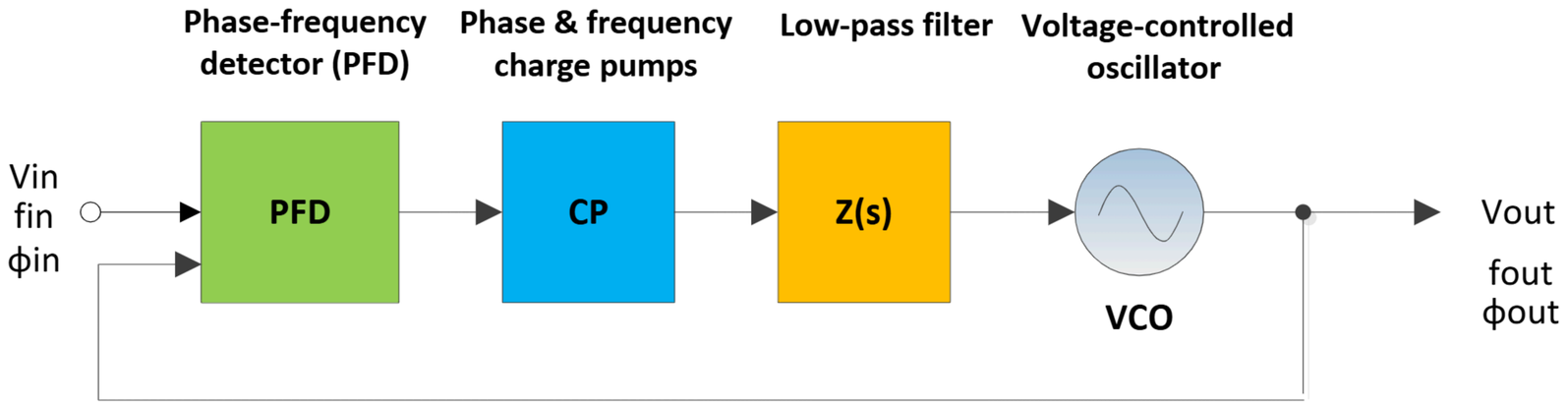
抖动指标

- CDR 能承受多少抖动压力
- 多少抖动会传播到其输出端

CDR 锁定行为

- 支持的数据速率
- 在运行条件下保持锁定一致性和稳定性

CDR lock acquisition in a retimer

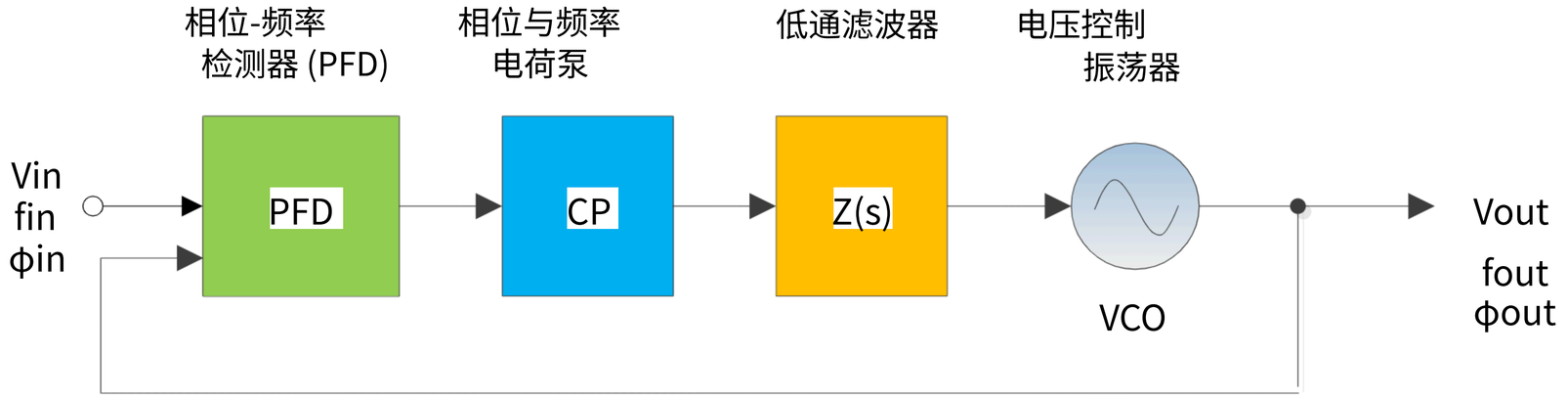


Type II PLL: phase and frequency detection

When the CDR is in locked condition, it meets the following criteria:

- Input and output phase are synchronized; $d\varphi_{out}/dt - d\varphi_{in}/dt = 0$ (φ is phase)
- $f_{out} = f_{in}$ (f is frequency)
  - f_{out} linearly tracks the control voltage (Vcont)
  - Average Vout that tracks small changes in input phase -> $\Delta\varphi$

在重定时器中的 CDR 锁定获取

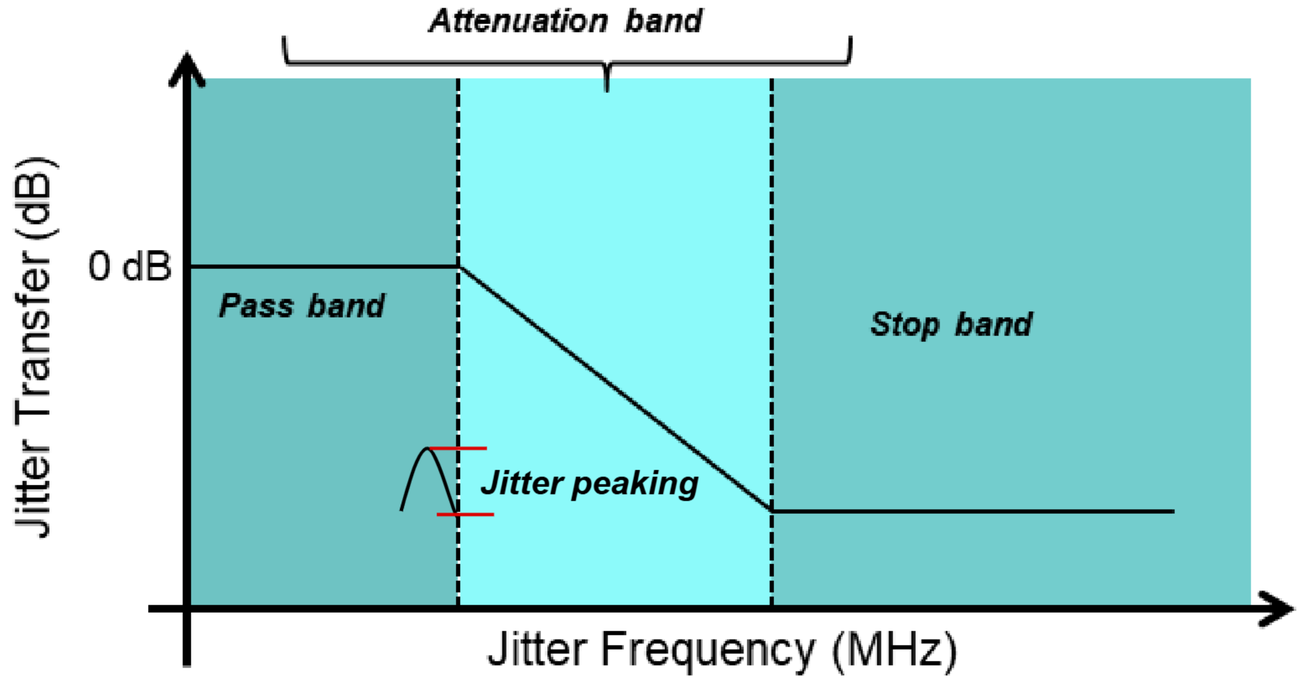


II 型 PLL：相位和频率检测

当 CDR 处于锁定状态时，它满足以下条件：

- 输入和输出相位同步；dϕ/dt - dϕ/dt = 0（ϕ是相位）
- $_{fout}$ = f（f 是频率）
  - $_{fout}$ 线性跟踪控制电压（Vcont）
  - 平均 Vout 跟踪输入相位的小变化 -> Δϕ

CDR metric: jitter transfer (JXFR)



Parameters of interest

- CDR loop bandwidth
- Pass band, attenuation band and stop band
- Jitter peaking

- Output jitter as a function of input jitter frequency
- May be expressed as: **JXFR = $|Jitter_{Out}(f) / Jitter_{in}|(f)|$**

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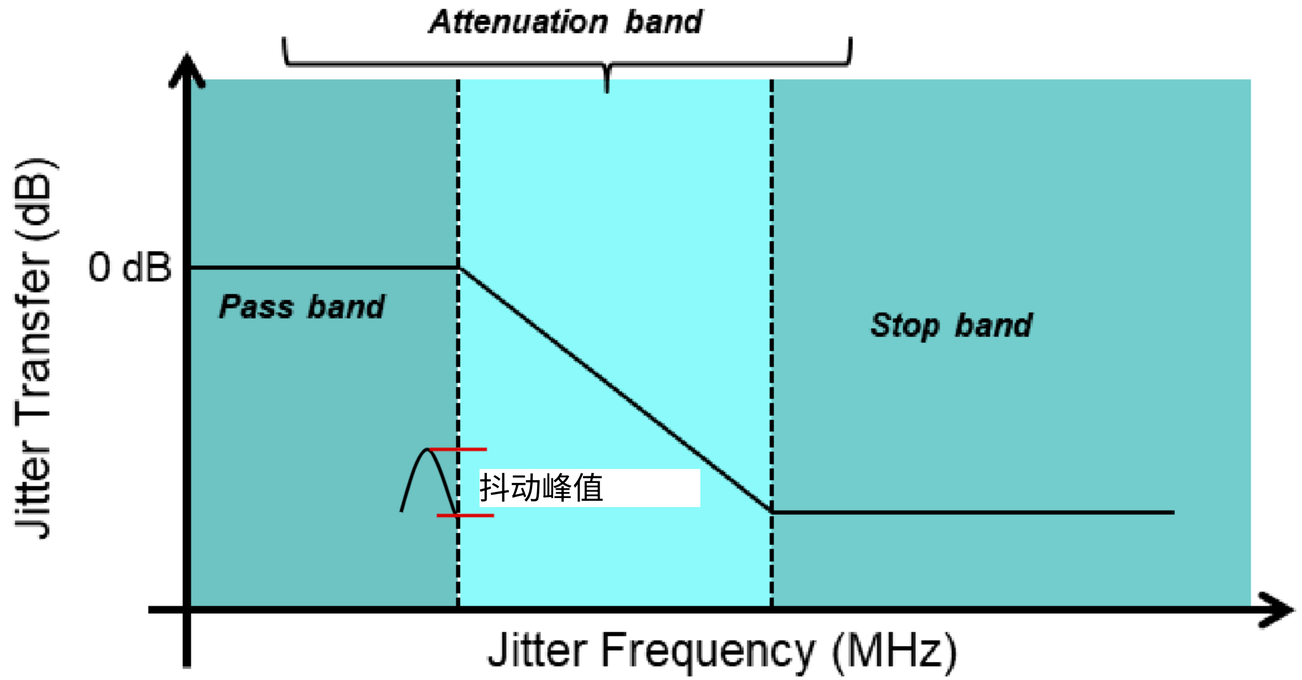
CDR 指标：抖动传输（JXFR）



感兴趣参数

- CDR 环路带宽
- 通带、衰减带和阻带
- 抖动峰值

- 输出抖动作为输入抖动频率的函数
- 可以表示为：JXFR = |Jitter(f)/ Jitter(f)|

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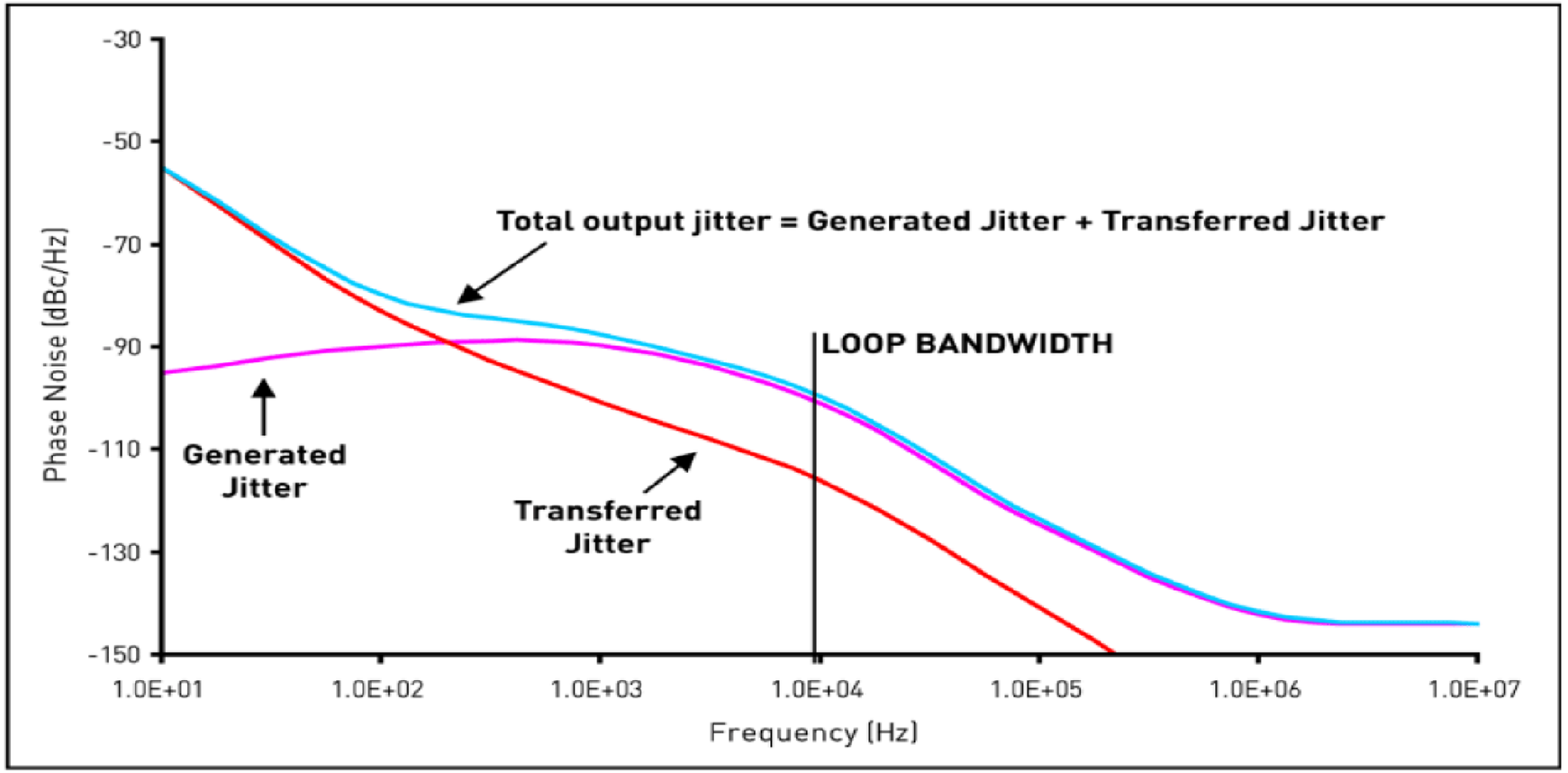
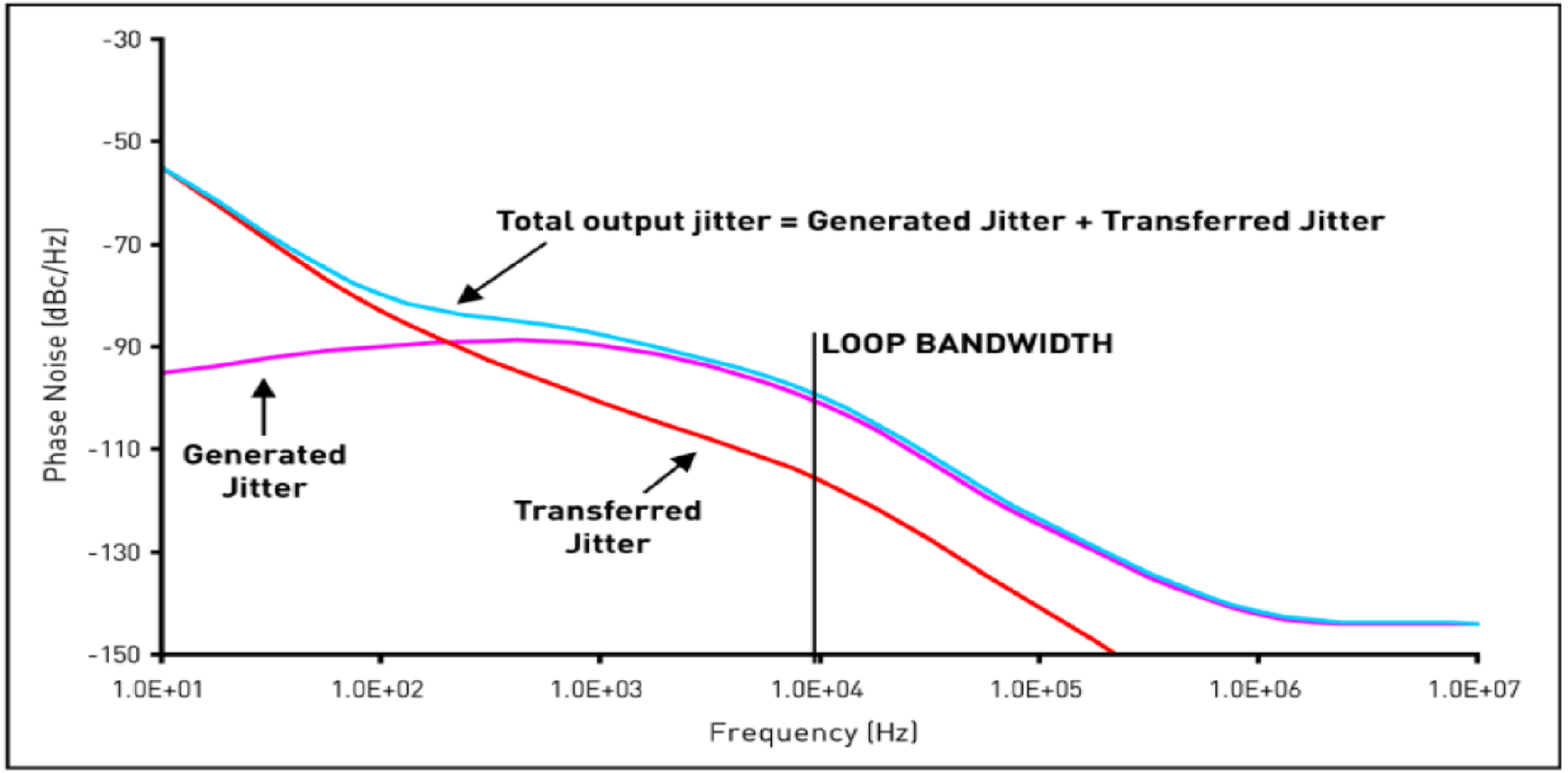
CDR metric: jitter generation



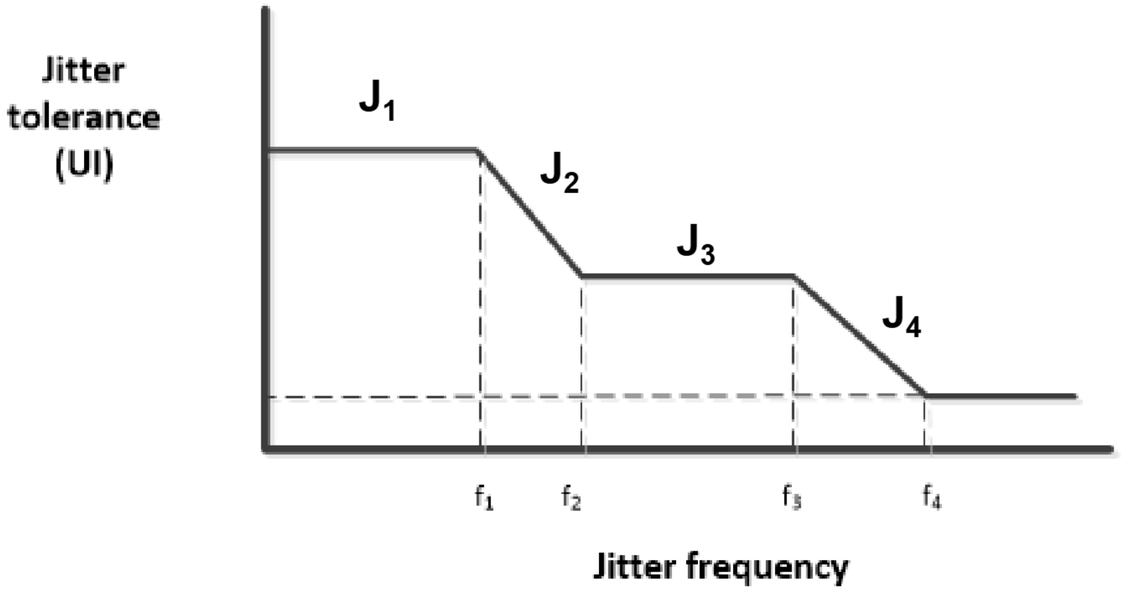
- Amount of output jitter for jitter free input data, as a function of frequency
- Jitter generation is a result of the CDR device intrinsic noise parameters

CDR 指标：抖动生成

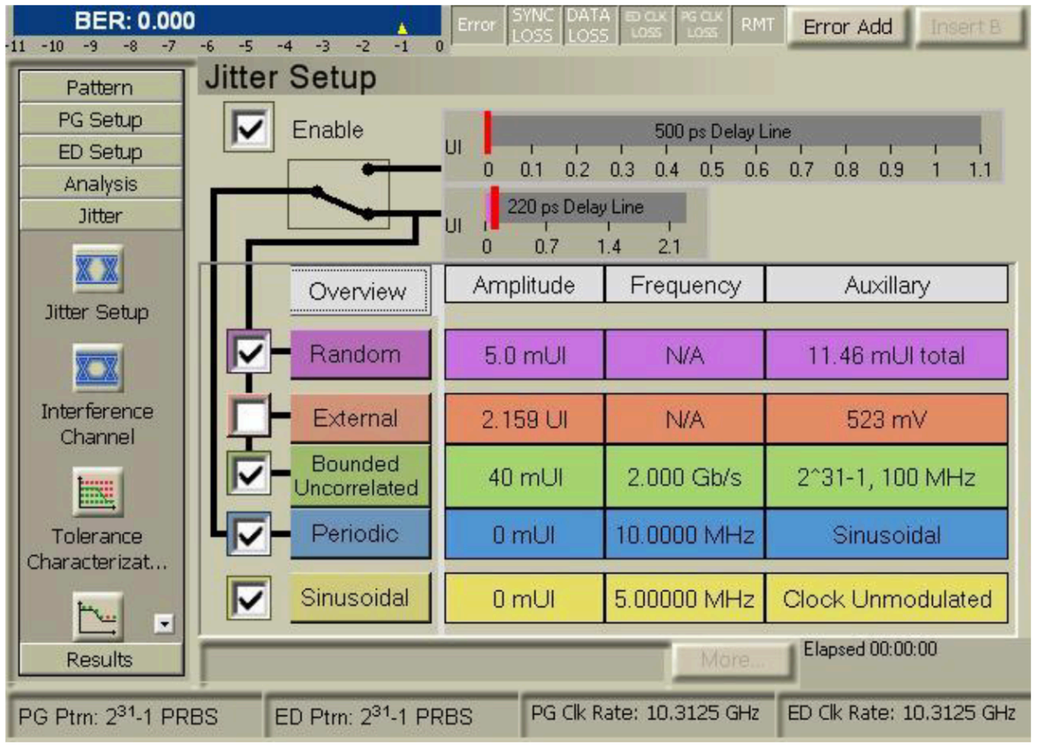


- 输出抖动量（针对无抖动输入数据），作为频率的函数
- 抖动产生是 CDR 设备固有噪声参数的结果

CDR metric: jitter tolerance (JTOL)



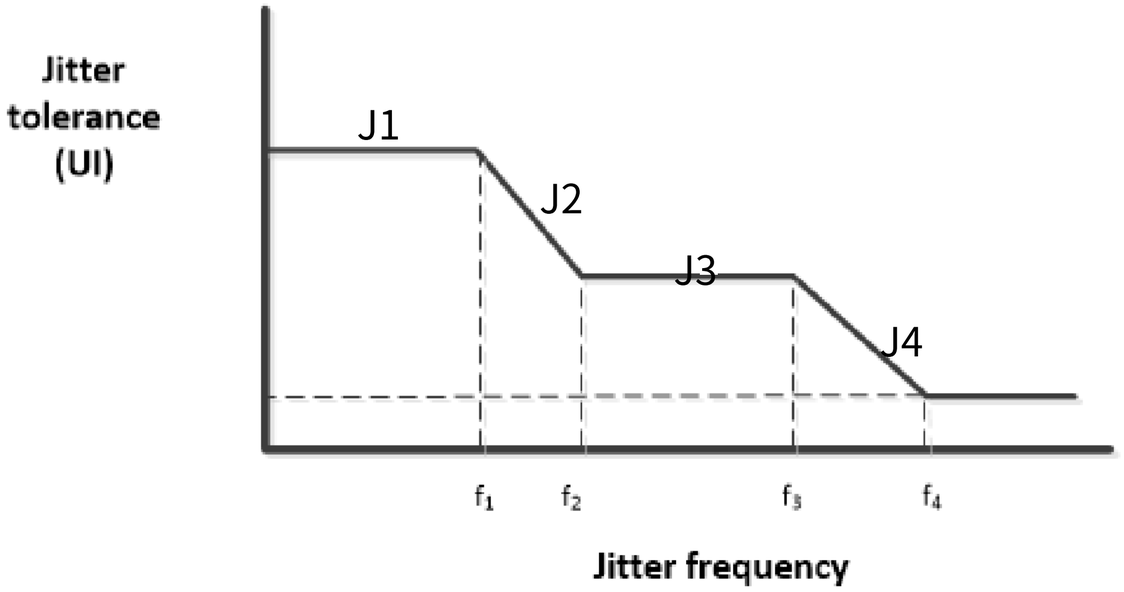
Representation of jitter tolerance mask used by standards



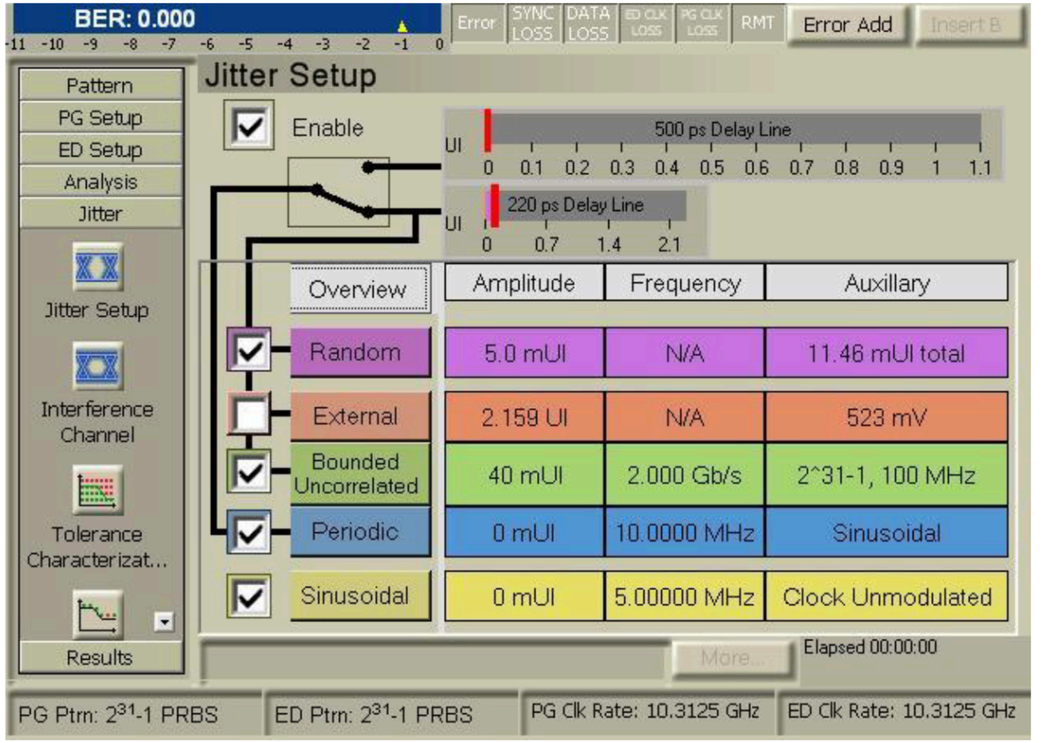
Example setup window for data generator with jitter stress

- Amount of input jitter that can be applied to the CDR without increasing bit error rate (BER)
- The higher the JTOL, the more link margin available to the system

CDR 指标：抖动容限（JTOL）



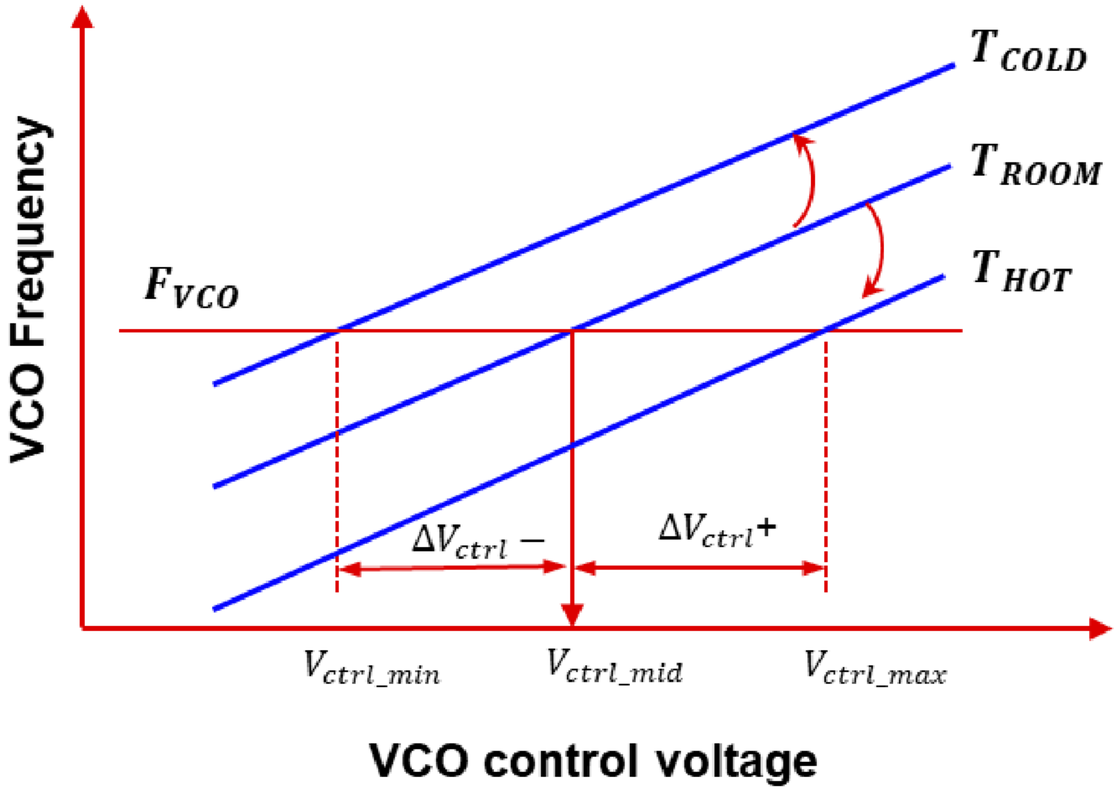
标准使用的抖动容限掩码表示



数据生成器的抖动应力示例设置窗口

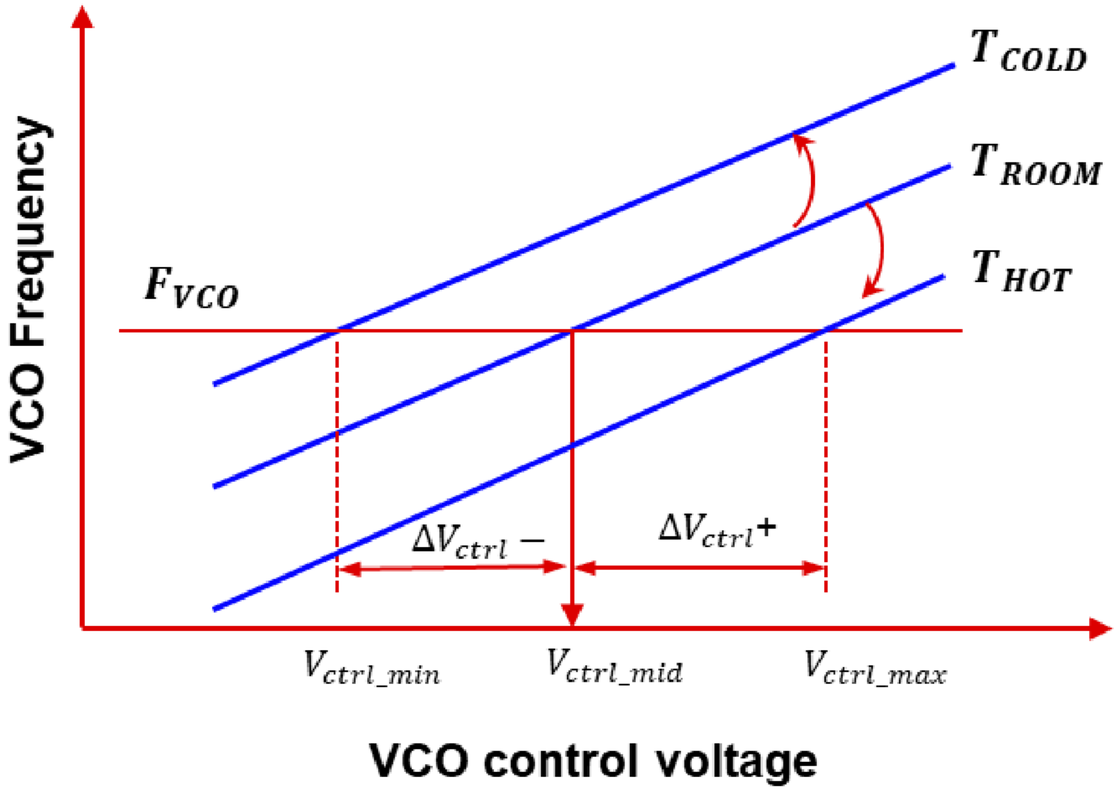
- 可应用于 CDR 而不会增加误码率（BER）的输入抖动量
- JTOL 越高，系统可用的链路裕量就越大

CDR metric: temperature lock range (TLR)



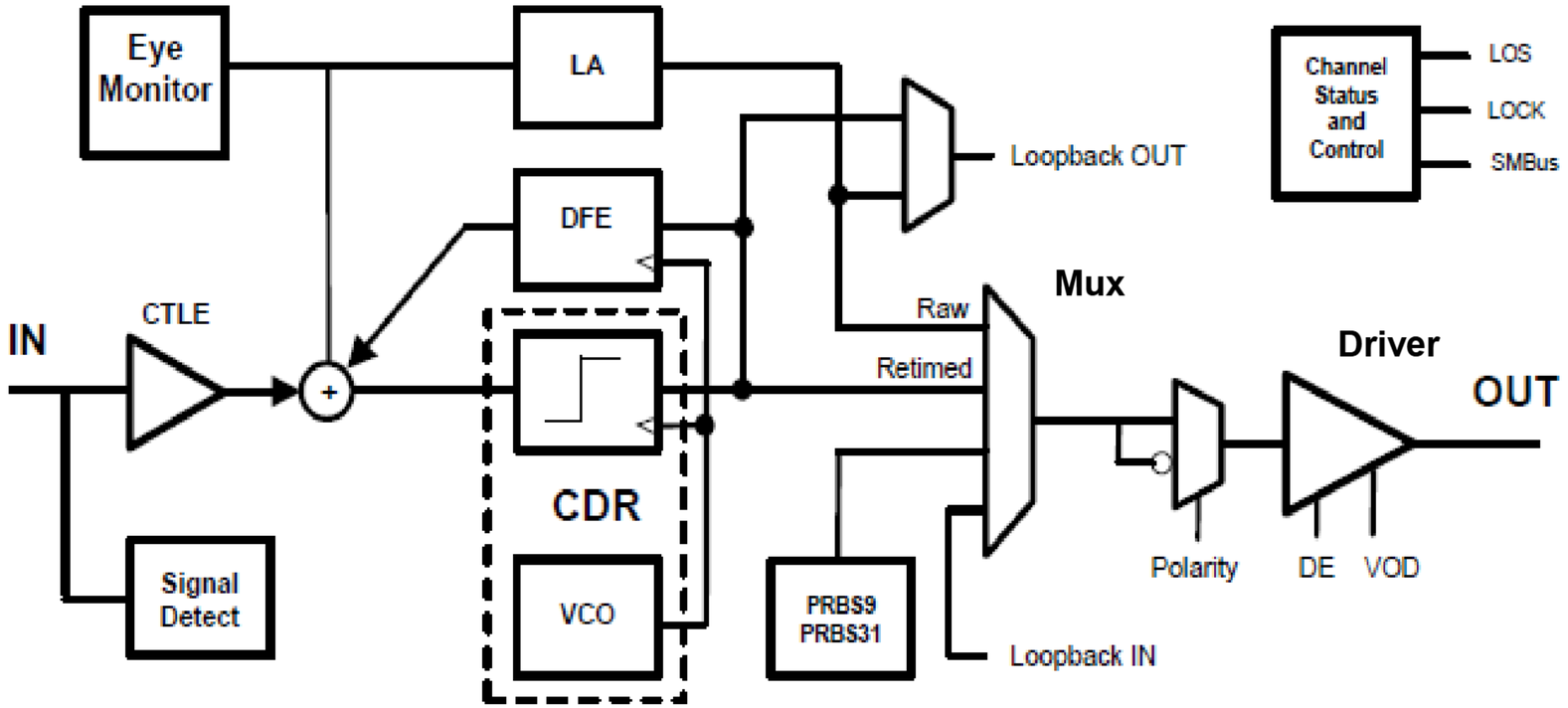
- TLR is the operating temperature range for which CDR can reliably maintain lock
- The larger the TLR, the more robust and versatile the retimer

CDR 指标：温度锁定范围（TLR）



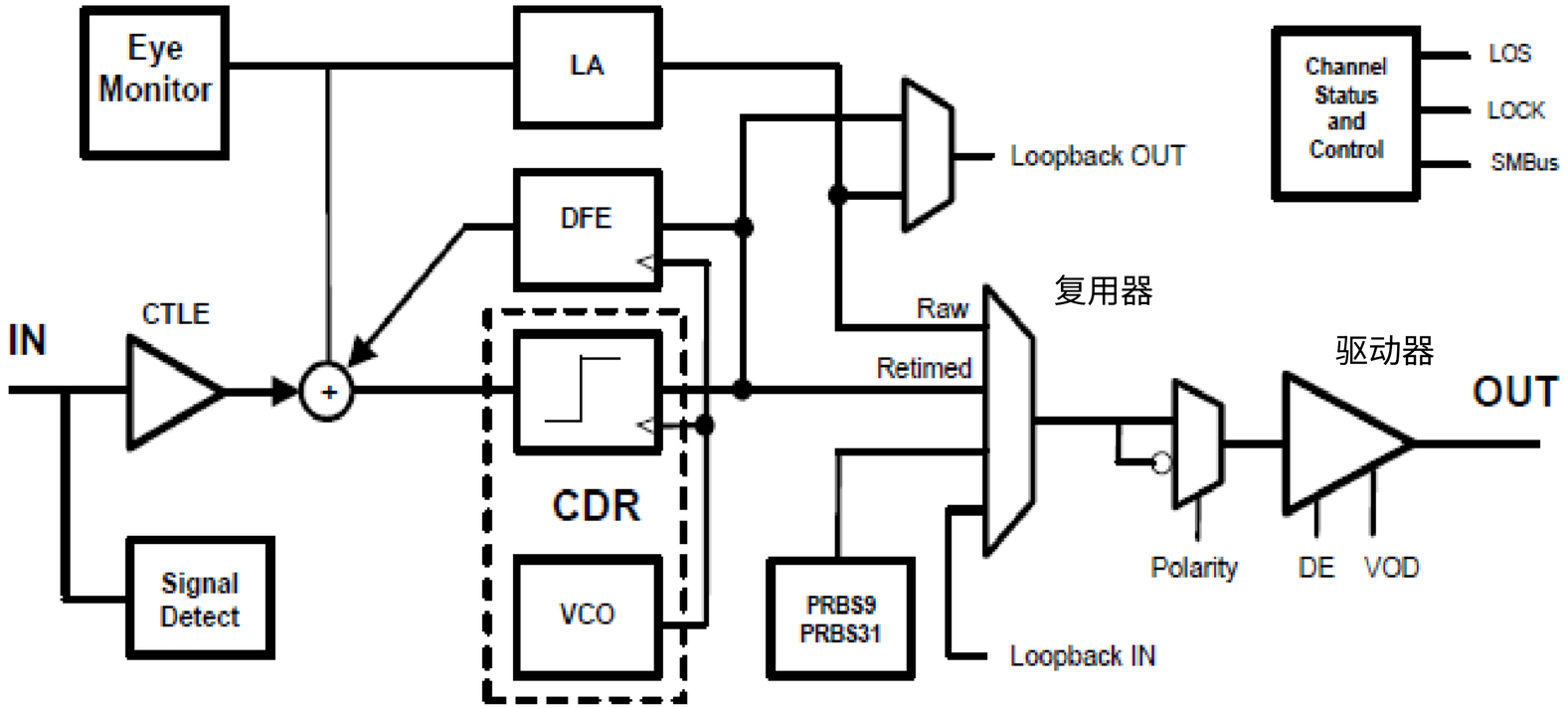
- TLR 是 CDR 能够可靠维持锁定的工作温度范围
- TLR 越大，重定时器就越鲁棒和通用

Functional block diagram of a 10Gbps retimer



In addition to the CDR, retimers may also implement input equalization, output equalization & system diagnostic features.

10Gbps 重新定时器的功能框图



除了 CDR，再定时器还可能实现输入均衡、输出均衡和系统诊断功能。